$3.00

Data Conversion Design Manual

TELEDYNE SEMICONDUCTOR

Teledyne Semiconductor — History

Early in 1961 a group of engineers and scientists, headed by Dr. Jay Last and Dr. Jean Hoerni, set out to establish their own firm. Last is holder of the patent for the metal-over-oxide technique and developer of the step and repeat camera. Hoerni is inventor and patent holder of the planar process.

The group was financed by Teledyne Inc., a systems company established a year earlier by Dr. Henry Singleton and Dr. George Kozmetsky. They became Amelco Semiconductor, division of Teledyne Inc., in February 1961.

The goals of Amelco were to develop highly reliable devices for special systems applications and Amelco was one of the first companies to produce and sell Junction Field Effect Transistors (JFETs) and High Noise Immunity Logic (HiNIL), products which Teledyne Semiconductor continues to produce.

In 1970 Amelco was merged with another division of Teledyne Inc. — Continental Devices Corp. — to form what is known today as Teledyne Semiconductor, Inc. Over the years Teledyne Semiconductor has grown to be an approved supplier to many high-reliability programs such as Apollo, Minuteman and Hawk.

The Specialist

Today Teledyne Semiconductor concentrates on producing:

- Junction Field Effect Transistors (JFETs)
- Bipolar Interface Logic
- Data Conversion Products (A/D, D/A, V/F, F/V, Voltage References, Multiplexers)
- FETRONs (Solid-State Replacements for Vacuum Tubes)

Teledyne Semiconductor's goal continues to be to supply reliable, quality products.

1980 Data Conversion Design Manual

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Teledyne Semiconductor assumes no responsibility for any circuits described in this manual and makes no representation that they are free from patent infringements. Teledyne Semiconductor reserves the right to update any portion of this manual without notification.

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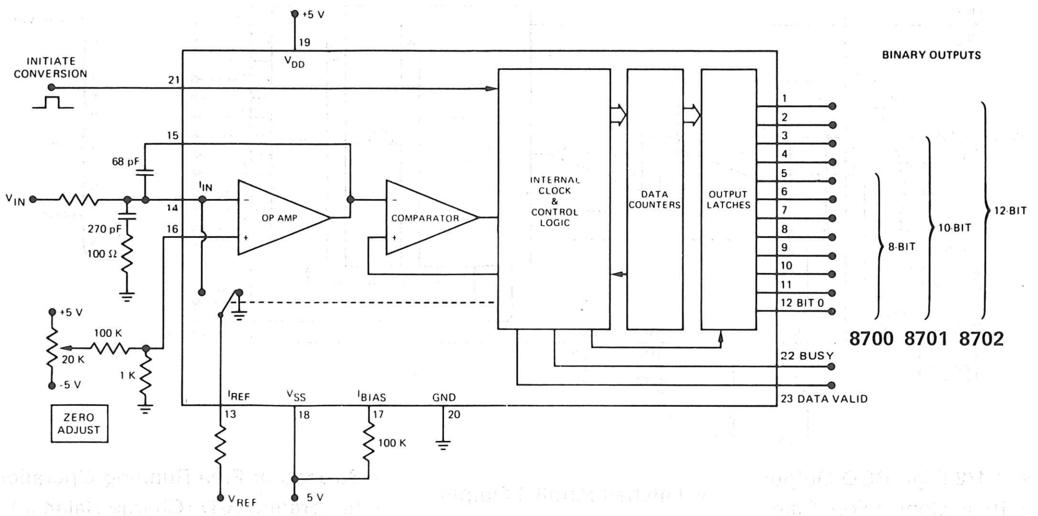
I

Introduction

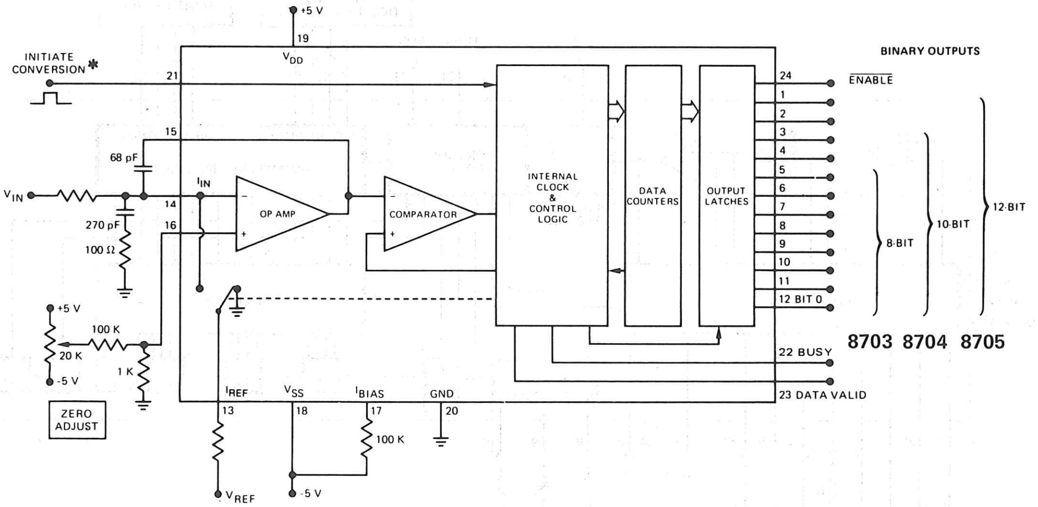
- Selector Guide
- Forthcoming Products
- Cross Reference Guide
- Quality and Reliability Programs

8700, 8701, 8702



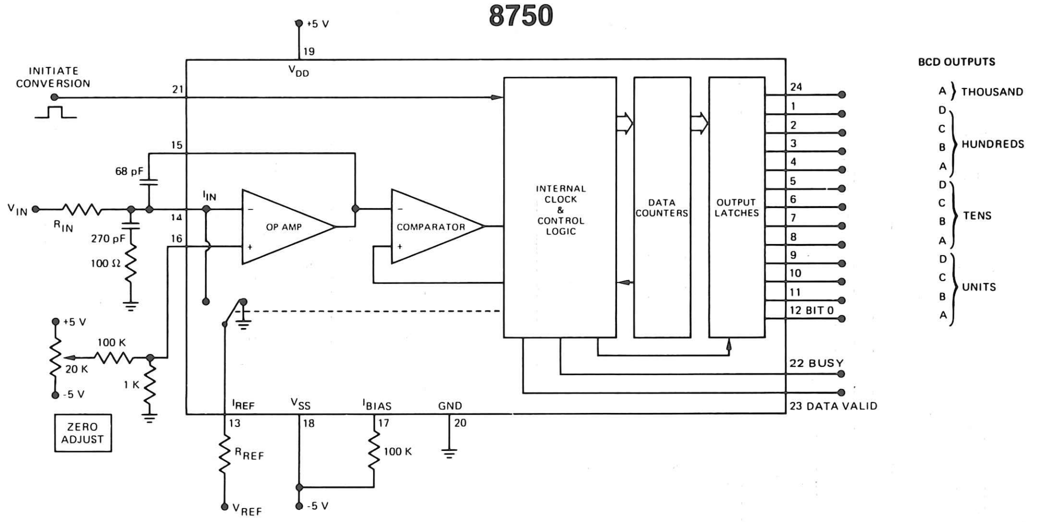
- 8, 10, or 12 Bit Binary Output
- 1 to 20ms Conversion Time
- Latched Parallel Output
- Strobed or Free Running Operation
- Integrating A/D (Charge Balance)

8703, 8704, 8705



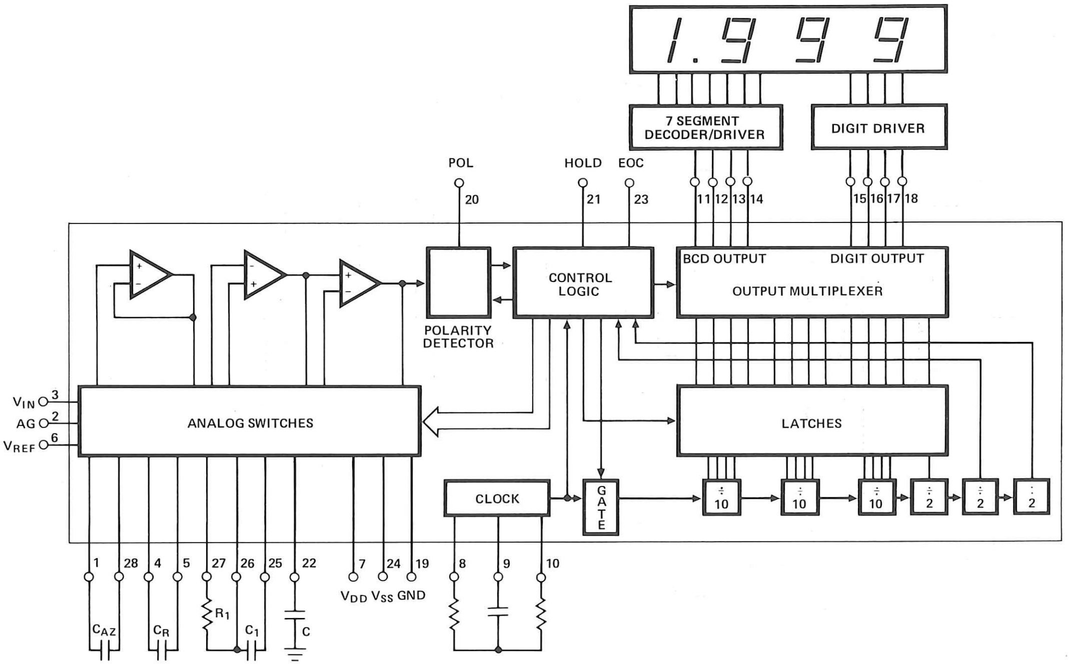
- 8, 10, or 12 Bit Binary Output
- 1 to 20ms Conversion Time
- Latched Three-State Outputs
- Strobed or Free Running Operation
- Integrating A/D (Charge Balance)

8750



- 3-1/2 Digit BCD Output
- 10ms Conversion Time
- Latched Parallel Output
- Strobed or Free Running Operation
- Integrating A/D (Charge Balance)

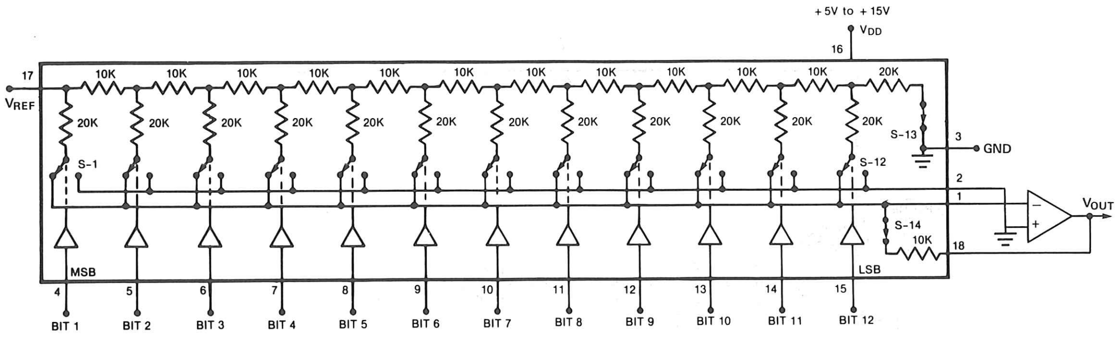
8751



- 3-1/2 Digit
- Auto Zero
- Multiplexed BCD Outputs
- Display Hold
- Auto Polarity
- Integrating A/D (Dual Slope)

D/A Converters

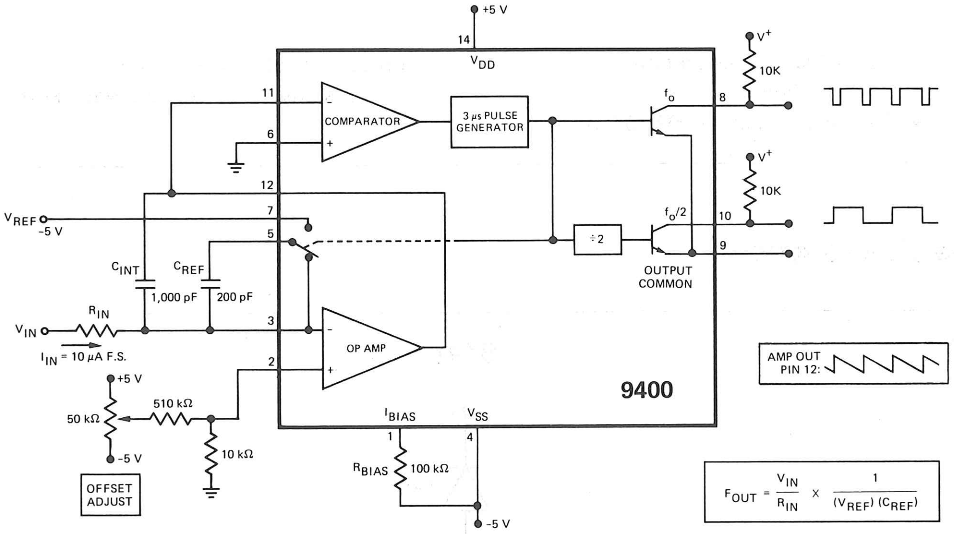
8640, 8641



- 12 Bit Binary
- 2ppm/° C Max. Gain Drift
- Choice of ±1/2 Bit or ±1 Bit Linearity
- Full Four Quadrant Multiplication
- 5V to 15V Operating Range

V/F, F/V Converters

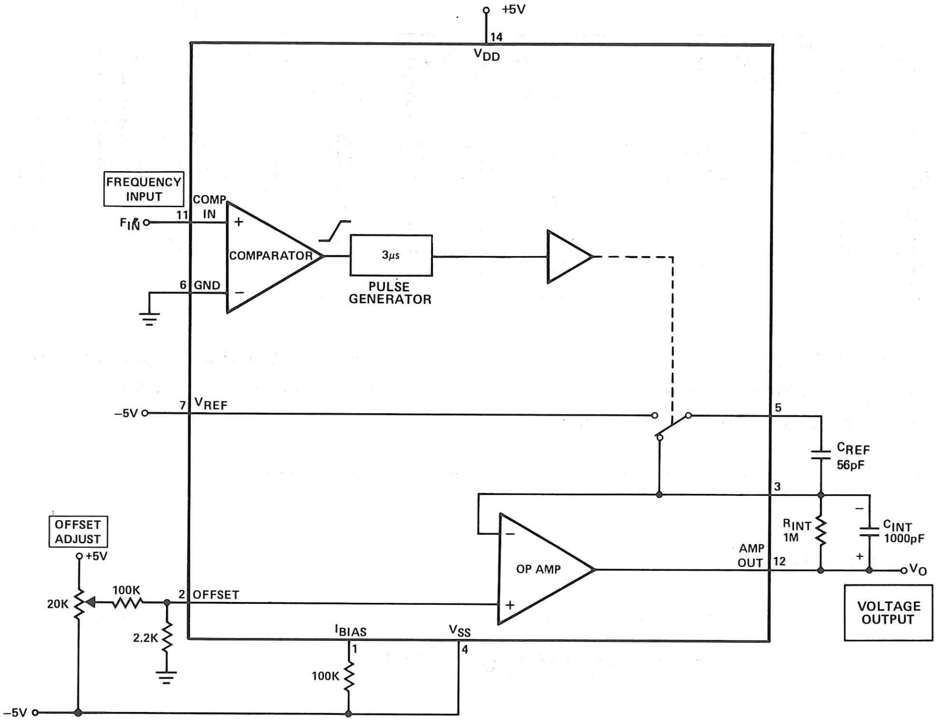
9400, 9401, 9402 V/F Mode



$$F_{OUT} = \frac{V_{IN}}{R_{IN}} \times \frac{1}{(V_{REF})(C_{REF})}$$

- 10 Hz to 100 KHz Operation
- 40ppm/° C Max. Gain Drift
- Choice of Linearity: .01, .05, or .25%
- Single or Dual Supply Operation
- Pulse and Square Wave Outputs

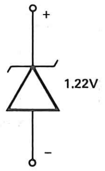
9400, 9401, 9402 F/V Mode



- DC to 100 KHz Operation
- Op Amp Output
- Choice of Linearity: .02, .05, or .25%
- Programmable Scale Factor
- Accepts any Input Voltage Wave Form

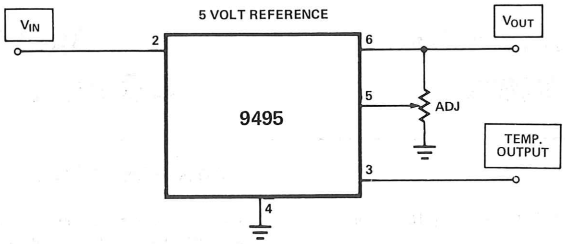
Voltage References

9491



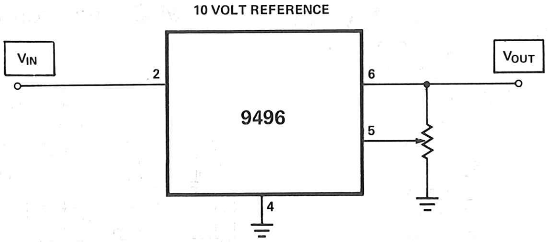
- 1.22V ± 2% Band Gap Reference
- 50 or 100ppm/°C Max. Temp Coefficient
- 50μA to 5mA Operating Range
- Low Output Noise — 5μV

9495



- 5V ± 0.3% or ±1% Band Gap Reference
- 8.5 or 65ppm/° C Max. Temp Coefficient
- 7V to 40V Input Voltage Range
- Temperature Output
- 10mA Output Current

9496



- 10V ±0.3% or ±1% Band Gap Reference
- 8.5 or 65ppm/° C Max. Temp. Coefficient
- 12V to 40V Input Voltage Range
- Low Noise — 30μVpp Max.
- 10mA Output Current

Monolithic CMOS A/D Converters

7106

3½ Digit Single Chip A/D For LCD Displays

PRELIMINARY

Features

Auto zero — guaranteed zero reading for 0 volts input on all scales.

Auto polarity.

True polarity at zero for precise null detection.

True differential input and reference.

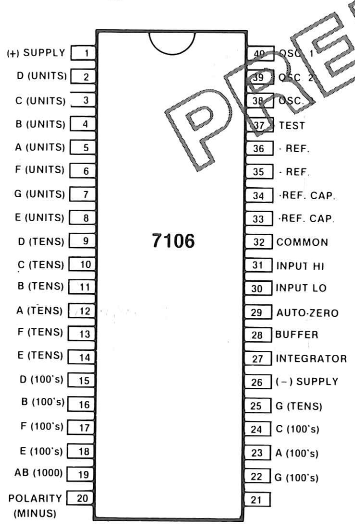
Direct drive to LCD display — no external components required.

On-chip clock and reference.

200.0 mV full scale sensitivity.

Direct replacement for Intersil 7106.

Pin Configuration

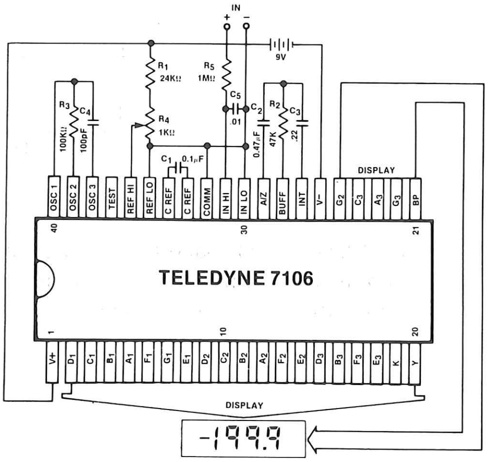


General Description

The Teledyne 7106 is a high performance, low power 3½ digit A/D converter. All the necessary active devices are contained on a single CMOS I.C., including seven segment decoders, display drivers, reference, and a clock. The 7106 is designed to interface with a liquid crystal display (LCD) and includes a backplane drive.

The 7106 brings together an unprecedented combination of high accuracy, versatility, and true economy. The versatility of true differential input and reference is useful in all systems, but gives the designer an uncommon advantage when measuring load cells, strain gauges and other bridge-type transducers. And finally the true economy of single power supply operation, enabling a high performance LCD panel meter to be built with the addition of only 7 passive components and a display.

Typical Connection Diagrams



A/D with Liquid Crystal Display

7107

Monolithic CMOS A/D Converters

3½ Digit Single Chip A/D For LED Displays

PRELIMINARY

Features

Auto zero — guaranteed zero reading for 0 volts input on all scales.

Auto polarity.

True polarity at zero for precise null detection.

True differential input and reference.

Direct drive to LED display — no external components required.

On-chip clock and reference.

200.0 mV full scale sensitivity.

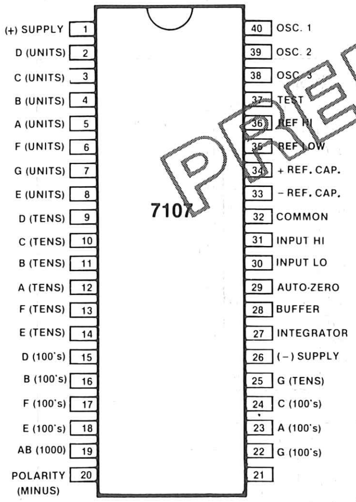
Direct replacement for Intersil 7107.

General Description

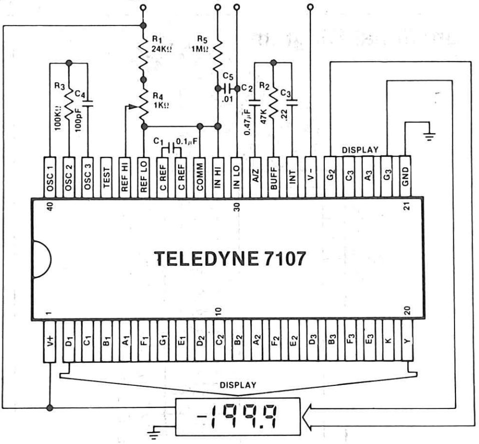
The Teledyne 7107 is a high performance, low power 3½ digit A/D converter. All the necessary active devices are contained on a single CMOS I.C., including seven segment decoders, display drivers, reference, and a clock. The 7107 will directly drive an instrument-size light emitting diode (LED) display.

The 7107 brings together an unprecedented combination of high accuracy, versatility, and true economy. The versatility of true differential input and reference is useful in all systems, but gives the designer an uncommon advantage when measuring load cells, strain gauges and other bridge-type transducers.

Pin Configuration



Typical Connection Diagrams



A/D with LED Display

Monolithic CMOS
Analog Multiplexer With Overload Protection

9486
16 Channel

Features

- Dielectrically Isolated CMOS
- $r_{ON} < 200\Omega$
- Analog Signal Range: ±15V
- Break-Before Make Switching
- TTL/DTL and CMOS Compatible
- Over Voltage and Power Loss Protected
- Low Power: 7.5mW
- Replaces DG506, HI-506A

Applications

- Data Acquisition
- Telemetry
- Industrial Control
- Switchable Gain Amplifier

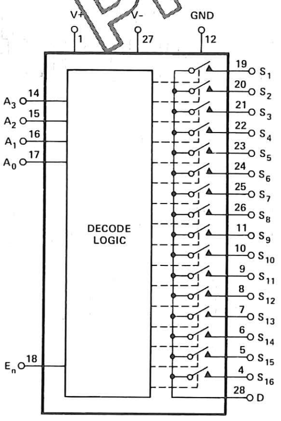
General Description

The Teledyne 9486 is a 16 channel dielectrically isolated CMOS analog multiplexer. Because of dielectric isolation, it can withstand analog input voltages much greater than the power supply voltage. This is very important in systems where the analog inputs originate from outside the equipment. The 9486 can also withstand continuous input voltages, even when the power supplies are turned off.

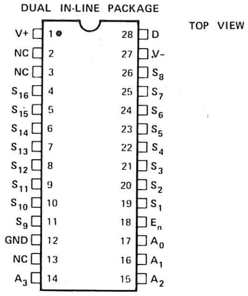
The 9486 employs 16 pairs of complimentary MOS (CMOS) field effect transistors to function as analog switches. In the ON condition, each switch will conduct current in either direction. The ON-OFF state of each switch is controlled by drivers which are in turn controlled by a 4-bit binary word input plus an enable-inhibit input. The Truth Table below shows the binary word required to select any one of the 16 switch positions, provided a logic "1" is present at the enable input. With a logic "0" at the enable input, all switches will be OFF.

PRELIMINARY

Functional Diagram



Pin Configuration



Decode Truth Table

A_3	A_2	A_1	A_0	E_n	"ON" SWITCH
X	X	X	X	0	NONE
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

Monolithic CMOS

Analog Multiplexer With Overload Protection

9487

Dual 8 Channel

PRELIMINARY

Features

- **Dielectrically Isolated CMOS**
- **$r_{ON} < 200\Omega$**
- **Analog Signal Range: ±15V**
- **Break-Before Make Switching**
- **TTL/DTL and CMOS Compatible**
- **Over Voltage and Power Loss Protected**
- **Low Power: 7.5mW**
- **Replaces DG507, HI-507A**

Applications

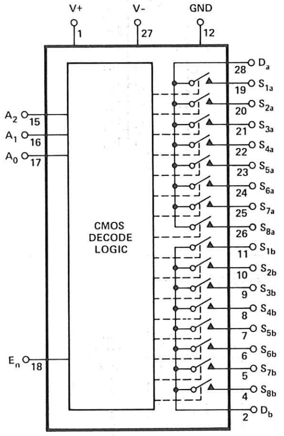
- **Data Acquisition**
- **Telemetry**
- **Industrial Control**
- **Switchable Gain Amplifier**

General Description

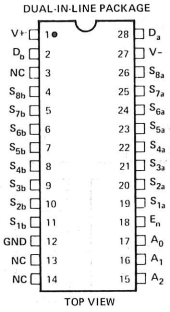
The Teledyne 9487 is a dual 8 channel dielectrically isolated CMOS analog multiplexer. Because of dielectric isolation, it can withstand analog input voltages much greater than the power supply voltage. This is very important in systems where the analog inputs originate from outside the equipment. The 9487 can also withstand continuous input voltages, even when the power supplies are turned off.

The 9487 employs 16 pairs of complimentary MOS (CMOS) field effect transistors to function as analog switches. In the ON condition, each switch will conduct current in either direction. The ON-OFF state of each switch is controlled by drivers which are in turn controlled by a 3-bit binary word input, plus an enable-inhibit input. The Truth Table below shows the binary word required to select any one of the 8 switch positions, provided a logic "1" is present at the enable input. With a logic "0" at the enable input, all switches will be OFF.

Functional Diagram



Pin Configuration



Decode Truth Table

A_2	A_1	A_0	E_n	"ON" SWITCH
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

Monolithic CMOS

Analog Multiplexer With Overload Protection

9488

8 Channel

Features

- Dielectrically Isolated CMOS
- $r_{ON} < 200\Omega$
- Analog Signal Range: ±15V
- Break-Before Make Switching
- TTL/DTL and CMOS Compatible
- Over Voltage and Power Loss Protected
- Low Power: 7.5mW
- Replaces DG508, HI-508A

Applications

- Data Acquisition
- Telemetry
- Industrial Control
- Switchable Gain Amplifier

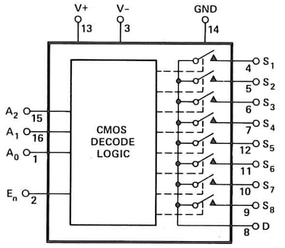
General Description

The Teledyne 9488 is an 8 channel dielectrically isolated CMOS analog multiplexer. Because of dielectric isolation, it can withstand analog input voltages much greater than the power supply voltage. This is very important in systems where the analog inputs originate from outside the equipment. The 9488 can also withstand continuous input voltages, even when the power supplies are turned off.

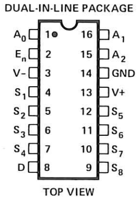
The 9488 employs 8 pairs of complimentary MOS (CMOS) field effect transistors to function as analog switches. In the ON condition, each switch will conduct current in either direction. The ON-OFF state of each switch is controlled by drivers which are in turn controlled by a 3-bit binary word input, plus an enable-inhibit input. The Truth Table below shows the binary word required to select any one of the 8 switch positions, provided a logic "1" is present at the enable input. With a logic "0" at the enable input, all switches will be OFF.

PRELIMINARY

Functional Diagram



Pin Configuration



Decode Truth Table

A_2	A_1	A_0	E_n	"ON" SWITCH
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

Monolithic CMOS

Analog Multiplexer
With Overload Protection

9489

Dual 4 Channel

Features

- Dielectrically Isolated CMOS
- $r_{ON} < 200\Omega$
- Analog Signal Range: ±15V
- Break-Before Make Switching
- TTL/DTL and CMOS Compatible
- Over Voltage and Power Loss Protected
- Low Power: 7.5mW
- Replaces DG509, HI-509A

Applications

- Data Acquisition
- Telemetry
- Industrial Control
- Switchable Gain Amplifier

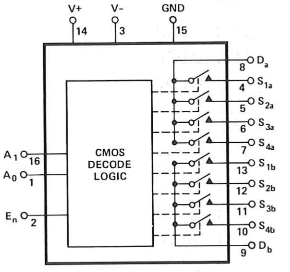
General Description

The Teledyne 9489 is a dual 4 channel dielectrically isolated CMOS analog multiplexer. Because of dielectric isolation, it can withstand analog input voltages much greater than the power supply voltage. This is very important in systems where the analog inputs originate from outside the equipment. The 9489 can also withstand continuous input voltages, even when the power supplies are turned off.

The 9489 employs 8 pairs of complimentary MOS (CMOS) field effect transistors to function as analog switches. In the ON condition, each switch will conduct current in either direction. The ON-OFF state of each switch is controlled by drivers which are in turn controlled by a 2-bit binary word input, plus an enable-inhibit input. The Truth Table below shows the binary word required to select any one of the 4 switch positions, provided a logic "1" is present at the enable input. With a logic "0" at the enable input, all switches will be OFF.

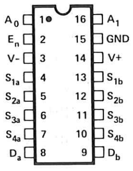
PRELIMINARY

Functional Diagram



Pin Configuration

DUAL-IN-LINE PACKAGE



TOP VIEW

Decode Truth Table

A_1	A_0	E_n	"ON" SWITCH PAIR
X	X	0	NONE
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

Cross Reference Guide

LISTED IN ALPHANUMERICAL ORDER

In all cases devices listed are considered exact replacements and are interchangeable. Direct replacements are based on similarity of electrical and mechanical characteristics as shown in currently published data. Interchangeability can not be guaranteed. Before using a device as a substitute, the user should compare specifications of the substitute device with those of the original.

Device. No.	Teledyne Semiconductor Device No.
AD7521LD	8640CN
AD7521LN	8640CJ
AD7521UD	8640BN
AD7531LD	8640CN
AD7531LN	8640CJ
AD7541AD	8640CN
AD7541BD	8641CN
AD7541JN	8640CJ
AD7541KN	8641CJ
AD7541SD	8640BN
AD7541TD	8641BN
ADC-EK8B	8700CJ
ADC-EK10B	8701CJ
ADC-EK12B	8702CN
ADC-EK12DC	8750CJ
ADC-EK12DM	8750BN
ADC-EK12DR	8750CN
ADC-ET8BC	8703CJ
ADC-ET8BM	8703BM
ADC-ET8BR	8703CN
ADC-ET10BC	8704CJ
ADC-ET10BM	8704BN
ADC-ET10BR	8704CN
ADC-ET12BC	8705CJ
ADC-ET12BM	8705BN
ADC-ET12BR	8705CN
DAC1220LCD	8640CJ
DAC1220LD	8640BN
ICL7112JJN	8640CN
ICL7112JPN	8640CJ
ICL7112KJN	8641CN
ICL7112KPN	8641CJ
ICL7112LPN	8641CJ
ICL7112SJN	8640BN
CIL7112TJN	8641BN
ICL8069CCQ	9491AJ
ICL8069CMQ	9491AM
ICL8069DCQ	9491BJ
ICL8069	9491BM
LM113	9491BM
LM313	9491BJ

Device No.	Teledyne Semiconductor Device No.
MP55010	9491BM
MP55010A	9491AM
MP5531AJ	9495AJ
MP5531BJ	9495AE
MP5531CJ	9495CE
MP5531DJ	9495CE
MP5531EJ	9495EJ
MP5531HJ	9495EE
MP5532AJ	9496AE
MP5532BJ	9496AE
MP5532CJ	9496CE
MP5532DJ	9496CE
MP5532EJ	9496EE
MP5532HJ	9496EE
MP713AD	8751CN
MP7137AN	8751CJ
MP7621AD	8640CN
MP7621BD	8641CN
MP7621JN	8640CJ
MP7621KN	8641CJ
MP7621SD	8640BN
MP7621TD	8641BN
REF-01AJ	9496AE
REF-01CJ	9496CE
REF-01CP	9496CJ
REF-01DJ	9496CE
REF-01DP	9496CJ
REF-01EJ	9496EE
REF-01HJ	9496EE
REF-01J	9496AE
REF-02AJ	9495AE
REF-02CJ	9495CE
REF-02CP	9495CJ
REF-02DJ	9495CE
REF-02DP	9495CJ
REF-02EJ	9495EE
REF-02HJ	9495EE
REF-02J	9495AE
VFQ1C	9400CJ
VFQ1R	9400CN
ZN423T	9491AJ
ZN423T	9491BJ

Cross Reference Guide

LISTED BY MANUFACTURER

In all cases devices listed are considered exact replacements and are interchangeable. Direct replacements are based on similarity of electrical and mechanical characteristics as shown in currently published data. Interchangeability can not be guaranteed. Before using a device as a substitute, the user should compare specifications of the substitute device with those of the original.

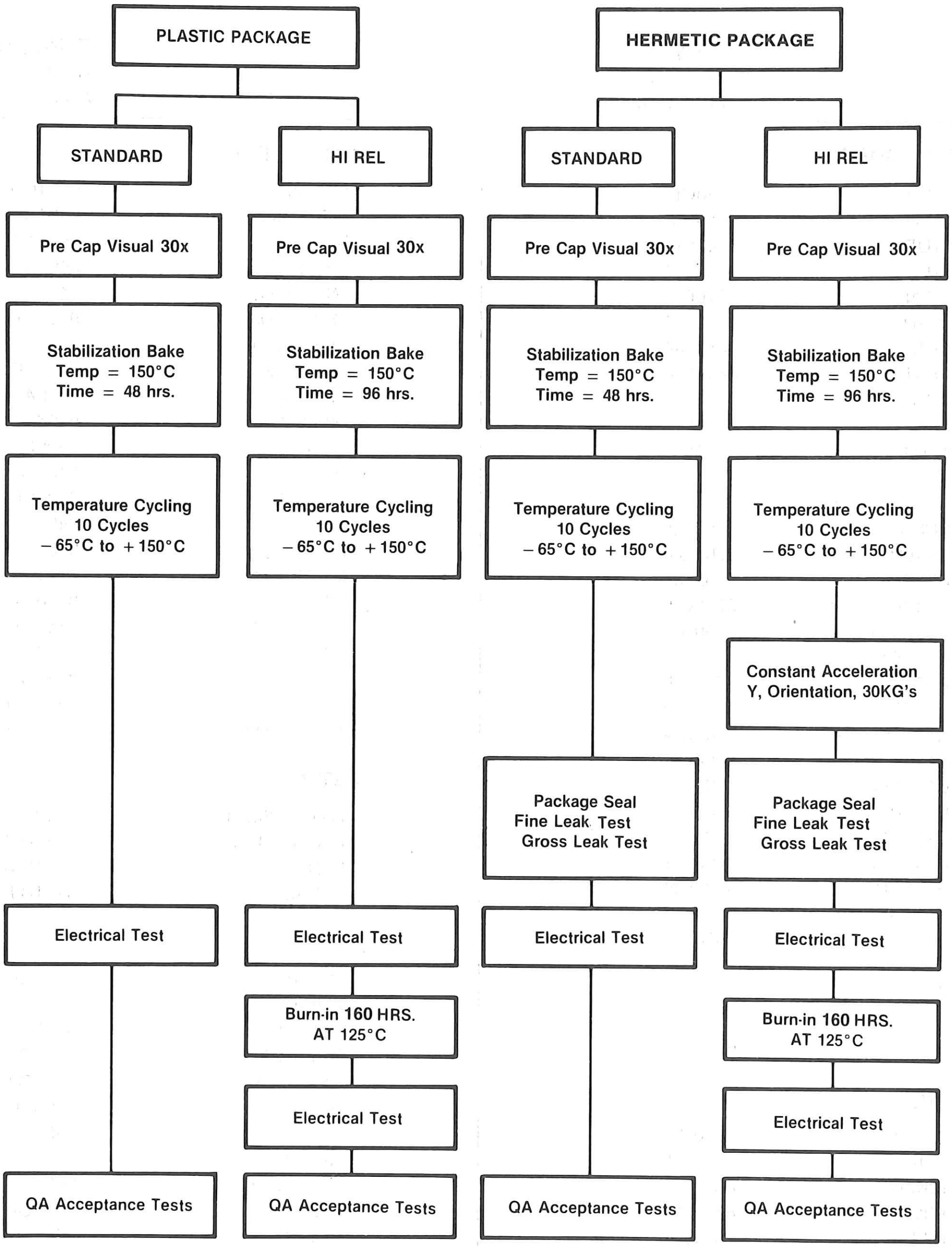
Device No.	Teledyne Semiconductor Device No.
ANALOG DEVICES	
AD7521LD	8640CN
AD7521LN	8640CJ
AD7521UD	8640BN
AD7531LD	8640CN
AD7531LN	8640CJ
AD7541AD	8640CN
AD7541BD	8641CN
AD7541JN	8640CJ
AD7541KN	8641CJ
AD7541SD	8640BN
AD7541TD	8641BN
DATEL	
ADC-EK8B	8700CJ
ADC-EK10B	8701CJ
ADC-EK12B	8702CN
ADC-EK12DC	8750CJ
ADC-EK12DM	8750BN
ADC-EK12DR	8750CN
ADC-ET8BC	8703CJ
ADC-ET8BM	8703BM
ADC-ET8BR	8703CN
ADC-ET10BC	8704CJ
ADC-ET10BM	8704BN
ADC-ET10BR	8704CN
ADC-ET12BC	8705CJ
ADC-ET12BM	8705BN
ADC-ET12BR	8705CN
VFQ1C	9400CJ
VFQ1R	9400CN
FERRANTI	
ZN423T	9491AJ
ZN423T	9491BJ
INTERSIL	
ICL7112JJN	8640CN
ICL7112JPN	8640CJ
ICL7112KJN	8641CN
ICL7112KPN	8641CJ
ICL7112LPN	8641CJ
ICL7112SJN	8640BN
ICL7112TJN	8641BN
ICL8069CCQ	9491AJ
ICL8069CMQ	9491AM
ICL8069DCQ	9491BJ
ICL8069	9491BM

Device No.	Teledyne Semiconductor Device No.
MICROPOWER	
MP55010	9491BM
MP55010A	9491AM
MP5531AJ	9495AJ
MP5531BJ	9495AE
MP5531CJ	9495CE
MP5531DJ	9495CE
MP5531EJ	9495EJ
MP5531HJ	9495EE
MP5532AJ	9496AE
MP5532BJ	9496AE
MP5532CJ	9496CE
MP5532DJ	9496CE
MP5532EJ	9496EE
MP5532HJ	9496EE
MP713AD	8751CN
MP7137AN	8751CJ
MP7621AD	8640CN
MP7621DB	8641CN
MP7621JN	8640CJ
MP7621KN	8641CJ
MP7621SD	8640BN
MP7621TD	8641BN
NATIONAL	
DAC1220LCD	8640CJ
DAC1220LD	8640BN
LM113	9491BM
LM313	9491BJ
PMI	
REF-01AJ	9496AE
REF-01CJ	9496CE
REF-01CP	9496CJ
REF-01DJ	9496CE
REF-01DP	9496CJ
REF-01EJ	9496EE
REF-01HJ	9496EE
REF-01J	9496AE
REF-02AJ	9495AE
REF-02CJ	9495CE
REF-02CP	9495CJ
REF-02DJ	9495CE
REF-02DP	9495CJ
REF-02EJ	9495EE
REF-02HJ	9495EE
REF-02J	9495AE

Quality and Reliability Programs

Integrated Circuit Screening

PER MIL-STD-883


PLASTIC PACKAGE
HERMETIC PACKAGE
STANDARD
HI REL
STANDARD
HI REL
Pre Cap Visual 30x
Pre Cap Visual 30x
Pre Cap Visual 30x
Pre Cap Visual 30x
Stabilization Bake Temp = 150°C Time = 48 hrs.
Stabilization Bake Temp = 150°C Time = 96 hrs.
Stabilization Bake Temp = 150°C Time = 48 hrs.
Stabilization Bake Temp = 150°C Time = 96 hrs.
Temperature Cycling 10 Cycles −65°C to +150°C
Temperature Cycling 10 Cycles −65°C to +150°C
Temperature Cycling 10 Cycles −65°C to +150°C
Temperature Cycling 10 Cycles −65°C to +150°C
Constant Acceleration Y, Orientation, 30KG's
Package Seal Fine Leak Test Gross Leak Test
Package Seal Fine Leak Test Gross Leak Test
Electrical Test
Electrical Test
Electrical Test
Electrical Test
Burn-in 160 HRS. AT 125°C
Burn-in 160 HRS. AT 125°C
Electrical Test
Electrical Test
QA Acceptance Tests
QA Acceptance Tests
QA Acceptance Tests
QA Acceptance Tests

Ordering Part Number:

XXXX AJ	XXXX AJ-101	XXXX AE	XXXX BN	XXXX AE-883B	XXXX BM-883B
XXXX BJ	XXXX BC-101	XXXX AM	XXXX CE	XXXX AM-883B	XXXX BN-883B
XXXX CJ	XXXX CJ-101	XXXX BH	XXXX CN	XXXX BH-883B	XXXX CN-883B
		XXXX BM	XXXX EE		

Quality and Reliability Programs

Product Assurance Program

The Quality Process

Teledyne Semiconductor has 16 years of experience in producing quality devices in a variety of product lines. Effective quality assurance, quality control, and reliability monitoring, along with built-in quality, have led to a consistently reliable product satisfying customer requirements. Such control and monitoring of manufacturing processes insures a quality product and consistent processes.

To this end, Teledyne Semiconductor views the quality process in four major blocks:

- Quality Control
- Quality Assurance
- Reliability
- Quality Control Circles

The Product Assurance Program

The program is based on MIL-Q-9858A requirements. Under the program, Teledyne Semiconductor manufactures devices for commercial and industrial users, and has total capability for complying with all requirements of MIL-M-38510, MIL-STD-19500, MIL-STD-883, MIL-STD-750, and MIL-STD-202. Teledyne Semiconductor is presently qualified to produce discrete JAN products.* Teledyne is also involved with various integrated circuit users on military programs.

The four aspects of the Product Assurance Program—Quality Control, Quality Assurance, Reliability and Quality Control Circles insure:

- Every method meets established standards (Quality Control)
- Every lot is checked to guaranteed parameters (Quality Assurance)
- The above are effective (Reliability)
- All workers are involved in quality and have a voice in their work (Quality Control Circles)

Quality Control

The Quality Control function handles continuous monitoring of production, from incoming inspection of raw materials to wafer and assembly processing. This includes surveillance of documentation, calibration, and environmental processing.

The three major areas of Quality Control are:

- Incoming Inspection
- In-Process Control
- Operation Surveillance

*Includes DESC acceptance of Teledyne Semiconductor's Quality Program at both the Mountain View and Hong Kong facilities.

Incoming Inspection

All purchased materials are inspected to criteria established internally based on finished product requirements. Control includes review by Quality Control of part drawings and purchase orders agreed to by suppliers.

Tests are performed on all direct material using a Lot Tolerance Percent Defective (LTPD) of 10% in accordance with MIL-S-19500. These test results are summarized monthly as part of a Vendor Rating System which evaluates each supplier's performance over a six month period. This evaluation aids Quality, Purchasing, and Engineering in determining what corrective action is necessary in order to achieve the desired incoming quality level.

In-Process Inspection

One of the most important aspects of the Product Assurance Program is the analysis and monitoring of virtually all production processes, equipment and devices. Process Control is divided into five major categories:

- Specification Review and Approval
- Process Audits
- Process Monitoring
- Process Gates
- Operator Certification

Every Teledyne Semiconductor generated specification is reviewed by a Quality Engineer to insure compliance to customer requirements as well as accuracy and workability of instructions. Key operations are audited periodically by the Quality Control Group to insure conformance to written instructions. The most vital of these operations is the Wafer Fabrication area. Here processes are audited daily and include checks on the operations, equipment and environment.

Environmental control involves close monitoring of temperature, relative humidity, water resistivity and bacteria content, as well as particle content in ambient air. All parameters are accurately controlled to minimize the possibility of contamination or adverse effects due to temperature or humidity excesses.

In addition to the specification conformance activities, the Quality Control group performs constant process monitoring at virtually every step. Results are supplied both to Manufacturing and Engineering, primarily in the form of trend charts. When evidence of a problem exists, Quality Control provides recommendations for correction and follows the corrective action taken.

Various process gates exist, primarily in the assembly area. All material subjected to manufacturing inspections is given to the Quality Control group for an independent sample. Quality Control limits are based on a 10% LTPD. If the sample is acceptable the material continues; if not, the material is sent back to manufacturing with a recommended disposition.

In the case of certain operations, it is more feasible for the Quality Control group to certify manufacturing operators, rather than continuously sample-inspect the material produced by that operator. The operator's work is inspected periodically and if it fails to meet established criteria, the operator is sent back for further training until ready for recertification.

Quality Assurance

The Quality Assurance (QA) function involves checking the ability of manufactured parts to meet specifications. In addition, the QA group is responsible for calibration of all equipment.

After devices are subjected to 100% testing in manufacturing, they are formed into lots and submitted to Quality Assurance acceptance testing. Three types of tests are performed on samples: Visual/Mechanical, Parametric, and Functional. The sampling is based on a 5% LTPD Plan. All testing is done at room and elevated temperature. Lower temperature testing is performed when required by the specification, or when a potential problem is known to exist.

To perform the electrical testing, QA uses test systems supplied by a variety of manufacturers, including in-house built testers and test fixtures.

If a lot is rejected by Quality Assurance, it is returned to manufacturing for rework or rescreen. Upon resubmission, a sample is pulled which is one level tighter than previously used. If the lot fails again, special disposition is made by QA and engineering which may include discarding the lot. In any event, corrective action by engineering is initiated.

An accepted lot is sent to packing and then to finished goods. When ready for shipment, the devices are submitted to a final Quality Assurance inspection where Visual/Mechanical tests are again performed. In addition, supporting documentation is verified, including QA acceptance, special customer requirements, and accuracy of the shipping paperwork.

Reliability

The Reliability Group is responsible for the following functions:

- New Process Qualification
- Process Change Qualification
- Process Monitoring
- New Device Qualification
- Device Change Qualification
- Device Monitoring
- New Package Qualification
- Package Change Qualification
- Package Monitoring
- Failure Analysis

Quality and Reliability Programs

The Reliability program at Teledyne Semiconductor involves initial qualification on any new designs, processes, or packages, or changes to existing ones. A decision matrix is documented and is used by Engineering to determine what areas might require qualification testing. Reliability Engineering is brought into the change loop early, and working with other engineers, a stress testing plan is devised. The data from this testing will help determine if the change will adversely affect long term reliability and the acceptability of the change is based on these test results.

In addition, the program includes scheduled requalification of existing devices, processes, and packages to insure controls are producing consistently reliable products.

Quality Control Circles

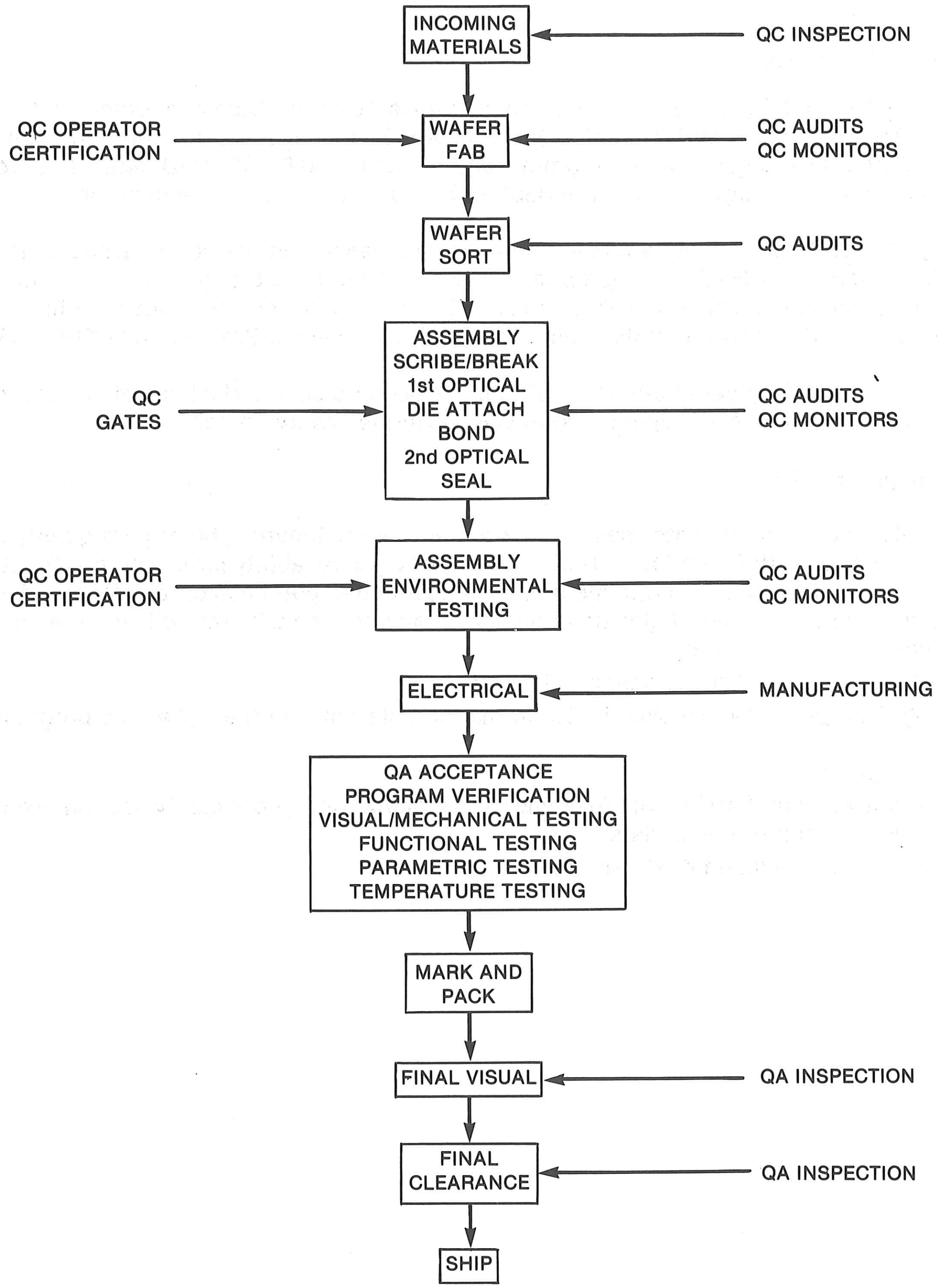
Quality Control Circles are becoming a vital part of the quality loop at Teledyne Semiconductor. The concept allows each employee, particularly those directly involved in manufacturing, to have a voice in how to build a quality product. Volunteers within a group meet weekly to determine and solve problems. The initial meetings are devoted to formal and rigorous training where the members are exposed to various tools for determining and solving problems. These techniques, such as brainstorming, data collection, and data graphing also help each person grow as an individual.

Some solutions to problems may be implemented on the job. Others require management support, and to this end, circle members are trained in management presentation. The goal is total employee involvement with an emphasis on building-in quality.

Summary

The Product Assurance Program is based on a close relationship between the Quality Group and the groups it services. Organizational structures do not become barriers. Quality is viewed as an attitude. The emphasis is on communication and problem solving as a team composed of professional experts in their field.

Product Assurance Program Implementation



High Reliability Products

JAN Qualified

The JAN qualified product is designed to give Teledyne Semiconductor customers the optimum in quality and reliability. The JAN processing level is the result of the government's product standardization programs, and is monitored by DESC (Defense Electronic Supply Center), through the use of industry-wide procedures and specifications.

JAN qualified products are manufactured, processed and tested in a DESC certified facility to MIL-STD-19500 and appropriate device slash sheets. Design documentation, lot sampling plans, electrical test data, and qualification data for each part type has been approved by DESC and products appear on the DESC Qualified Products List (QPL-19500).

Group B testing per MIL-STD-19500 and the specific device slash sheet is performed on each lot for each slash sheet. Group C is performed every six months.

Generic Data

Teledyne Semiconductor has a new program for customers who require quality conformance data on their products. This program provides reliability information without the necessity of running Group B inspections for a particular purchase order. Generic data is generated on a three month (maximum) basis in accordance with the following table, and is compiled from data on:

(1) JAN Quality Conformance Lots, and

(2) Data generated by Quality Conformance Lots run for other reliability programs.

This program:

- Allows qualification of Teledyne Semiconductor's products based on existing quality conformance data
- Provides reduced costs and improved delivery.

II

Monolithic CMOS A/D Converters

8700 — 8705, 8750
A/D Converters Summary Data

CONVERSION PRINCIPLE — "Incremental Charge Balance" Technique integrates the input for noise rejection.

		8-bit	10-bit	12-bit	3½ digit
CONVERSION RATE	—	800 cps	200 cps	50 cps	100 cps
CONVERSION TIME	—	1.25 ms	5 ms	20 ms	10 ms

CONVERSION MODE — Free Run: Pin 21 tied to V_{DD}.
Initiate On Command: Positive Pulse on Pin 21 (500 ns Min Pulse Width).

SUPPLY
- — V_{DD}: 3.5V to 7.0V — V_{SS}: −3.5V to −7.0V
- — I_{DD}: 1.4ma — I_{SS}: −1.6ma

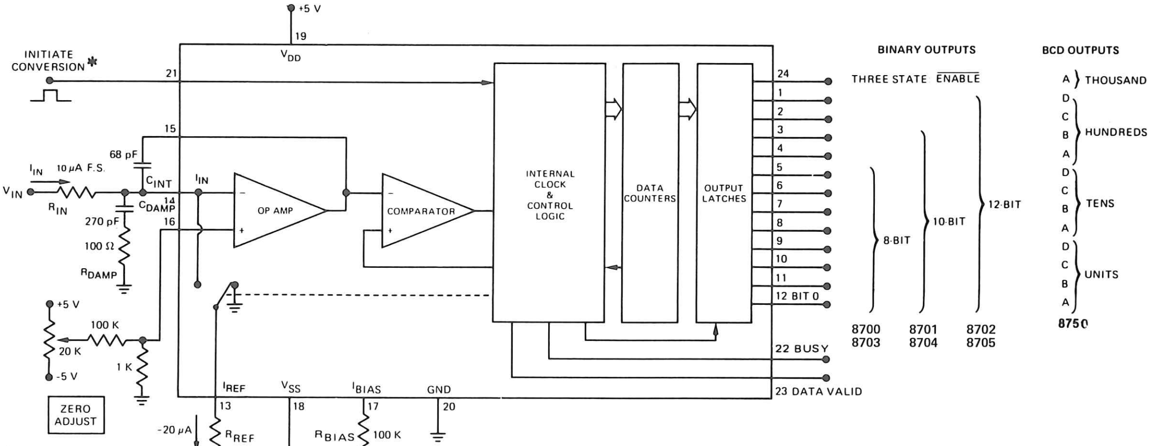
OUTPUTS
- — Data is latched in a parallel format (non-multiplexed).
- — Drives: Two low-power gates (500μA sink at V_{OL} = 0.4).
  CMOS (Fan Out of 10).

INPUTS
- — +10μA for Full Scale Output (scale any positive input voltage with an input resistor).
- — −20μA Reference Current (scale any negative voltage with a reference resistor.)
- — Effect of Over-Voltage: None, for I_{IN} < 1ma. (Output stays at Full Scale.)
- — Effect of Under-Voltage: None, for I_{IN} < 1ma. (Output reading is 0000.)
- — For Bipolar (±) Inputs, use an Offset Resistor or an Absolute Value Circuit.

TEMPERATURE STABILITY
- — Zero Point: ±30μV/°C
- — Full Scale/Gain: ±25ppm/°C (±0.0025%/°C)

ACCURACY — ± ½ Bit

R_{BIAS}
- — Controls conversion time (permitting 50/60Hz conversion rate on 12-Bit for line rejection. 3 to 1 change is possible (see AN-9).
- — Affects op Amp Gain
- — Determines I_{DD}, I_{SS} current



*Tie to V_{DD} for free run mode
V_{DD}, V_{SS}: 3.5V to 7.0V

Monolithic CMOS A/D Converters

8700 Series

8700, 8701, 8702

8,10,12 Bit

Binary

Features

High Accuracy — Up to 12 Bit Resolution with < ±½ LSB Error

Monotonic Performance — No Missing Codes

Monolithic CMOS Construction Gives Low Power Dissipation — 20mW Typical

Contains All Required Active Elements — Needs Only Passive Support Components, Reference Voltage And Dual Power Supply

High Stability Over Full Temperature Range
- Gain Temperature Coefficient Typically <25ppm/°C
- Zero Drift Typically $<30\mu V/°C$
- Differential Non-Linearity Drift Typically <2.5ppm/°C

Latched Parallel Binary Outputs

LPTTL And CMOS Compatible Outputs And Control Inputs

Strobed Or Free Running Conversion

Infinite Input Range — Any Positive Voltage Can Be Applied Via A Scaling Resistor

Absolute Maximum Ratings

Storage Temperature		−65°C to +150°C
Operating Temperature	(N Package)	−40°C to +85°C
	(J Package)	0°C to 70°C
$V_{DD} - V_{SS}$		18V
I_{IN}		±10mA
I_{REF}		±10mA
Digital Input Voltage		−0.3 to V_{DD} +0.3V
Operating V_{DD} and V_{SS} Range		**3.5V to 7V**
Package Dissipation		500mW
Lead Temperature (Soldering, 10 seconds)		300°C

HANDLING PRECAUTIONS

The 8700 series are CMOS devices and must be handled correctly to prevent damage. Package and store only in conductive foam, anti-static tubes or other conductive material. Use proper anti-static handling procedures. Do not connect in circuits under "power on" conditions, as high transients may cause permanent damage.

General Description

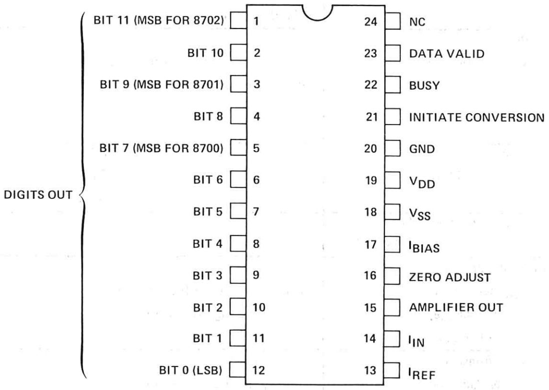
The Teledyne Semiconductor 8700/8701/8702 are 8/10/12 bit monolithic CMOS analog-to-digital converters. Fully self-contained in a single 24-pin dual in-line package, each converter requires only passive support components, voltage or current reference and power supplies.

Conversion is performed by an incremental charge balancing technique which has inherently high accuracy, linearity and noise immunity. An amplifier integrates the sum of the unknown analog current and pulses of a reference current, and the number of pulses (charge increments) needed to maintain the amplifier summing junction near zero is counted. At the end of conversion the total count is latched into the digital outputs as an 8/10/12 bit binary word.

Connection Diagram

Order Part Numbers:

N Package	J Package
24-Pin Ceramic DIP	**24-Pin Plastic DIP**
(−40°C to +85°C)	**(0°C to 70°C)**
8700CN — 8 bit	8700CJ — 8 bit
8701CN — 10 bit	
8702CN — 12 bit	



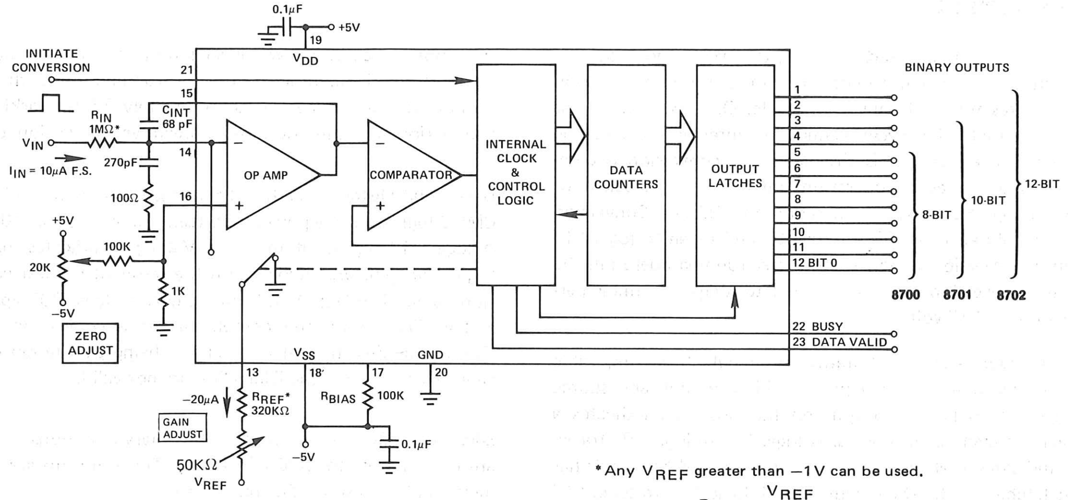
NOTE: Pin 1 indicated by adjacent dot or indent (N package), or end notch (J package). Do not make connections to pin 1, 2, 3 or 4 on 8700; pin 1 or 2 on 8701. These pins are internally connected.

Electrical Characteristics Unless otherwise specified, $V_{DD} = +5V$, $V_{SS} = -5V$, $V_{GND} = 0$, $V_{REF} = -6.4V$, $R_{BIAS} = 100K\Omega$, test circuit shown. $T_A = 25°C$ unless Full Temp. Range is specified (−40°C to +85°C for N package, 0°C to 70°C for J package).

Parameter	Definition	Min	Typ	Max	Units	Conditions
Accuracy						
Resolution Accuracy	Binary word length of digital output					
	8700	8			Bits	
	8701	10			Bits	
	8702	12			Bits	
Relative Accuracy	Output deviation from straight line between normalized zero and full scale input			±1/2	LSB	
Differential Non-Linearity	Deviation from 1 LSB between transition points		±1/4	±1/2	LSB	
Differential Non-Linearity Temperature Drift	Variation in Differential Non-Linearity due to temperature change		±2.5	±5	ppm/°C	Full Temp. Range
Gain Variance	Variation from exact A (compensate by trimming R_{IN} or R_{REF})		±2	+5 −3	% of Nominal	
Gain Temperature Drift	Variation in A due to temperature change		±25	±75	ppm/°C	Full Temp. Range
Zero Offset	Correction at zero adjust to give zero output when input is zero		±10	±50	mV	$I_{IN} = 0$
Zero Temperature Drift	Variation in zero offset due to temperature change		±30	±50	μV/°C	Full Temp. Range
Analog Inputs						
I_{IN} Full Scale	Full scale analog input current to achieve specified accuracy		10		μA	
I_{REF} (Note 1)	Reference current input to achieve specified accuracy		−20		μA	
Digital Inputs						
V_{IN} (1)	Logical "1" input threshold for Initiate Conversion Input	3.5			V	Full Temp. Range
V_{IN} (0)	Logical "0" input threshold for Initiate Conversion input			1.5	V	Full Temp. Range
Digital Outputs						
V_{OUT} (1)	Logical "1" output voltage for Digits Out, Busy, and Data Valid Outputs					Full Temp. Range
		4.5			V	$I_{OUT} = -10\mu A$
		2.4			V	$I_{OUT} = -360\mu A$
V_{OUT} (0)	Logical "0" output voltage for Digits Out, Busy, and Data Valid Outputs			0.4	V	Full Temp. Range $V_{DD} = 4.75V$, $I_{OUT} = 360\mu A$
Dynamic						
Conversion Time	Time required to perform one complete A/D conversion 8700		1.25	1.8	ms	Full Temp. Range
	8701		5	6	ms	
	8702		20	24	ms	
Conversion Rate in Free-Run Mode	8700	555	800		Conv'ns per Second	$V_{INIT\ CONV} = +5V$
	8701	167	200			
	8702	42	50			
Minimum Pulse Width for Initiate Conversion		500			ns	Full Temp. Range
Supply Current						
I_{DD} Quiescent	Current required from positive supply during operation					
(N Package)			1.4	2.5	mA	Full Temp. Range $V_{INIT\ CONV} = 0V$
(J Package)			1.4	5.0	mA	
I_{SS} Quiescent	Current required from negative supply during operation					
(N Package)			−1.6	−2.5	mA	
(J Package)			−1.6	−5.0	mA	
Supply Sensitivity	Change in full scale gain vs supply voltage change		±0.5	±1.0	%/V	$V_{DD} \pm 1V$, $V_{SS} \pm 1V$
	Change in full scale gain vs supply voltage change for tracking supplies		±0.05	±0.1	%/V	$\lvert V_{DD}\rvert = \lvert V_{SS}\rvert = 5V \pm 1V$

NOTE: I_{IN} and I_{REF} pins connect to the summing junction of an operational amplifier. Voltage sources cannot be attached directly but must be buffered by external resistors. See Test Circuit.

Test Circuit



*Any V_{REF} greater than –1V can be used.

$$R_{REF} = \frac{V_{REF}}{-20\mu A}$$

For example with V_{REF} = –5V, R_{REF} = 250K.

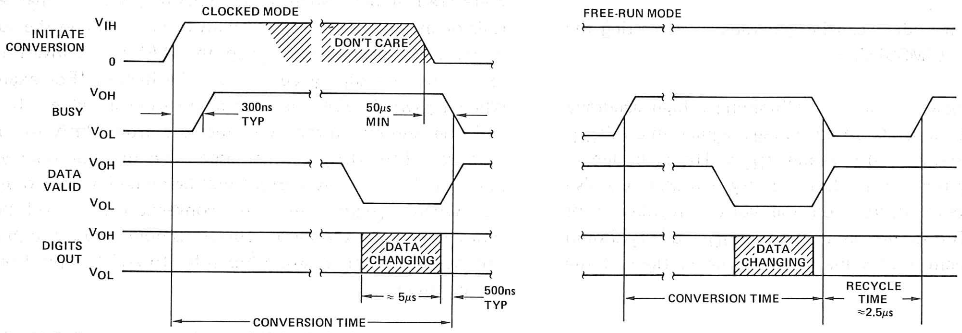
Circuit Description

During conversion the sum of a continuous current I_{IN} and pulses of a reference current I_{REF} is integrated for a fixed number of clock periods. I_{IN} is proportional to the analog input voltage; I_{REF} is proportional to the reference voltage and is of opposite sign to I_{IN}. I_{REF} is switched in for exactly one clock period just frequently enough to maintain the summing input of the integrator near zero. Thus, the charge from the continuous I_{IN} current is balanced against the pulses of I_{REF} current. The total number of I_{REF} pulses needed during the conversion period to maintain the charge balance is counted, and the result (in binary) is latched into the outputs at the end of conversion.

The converter contains two counters and a clock in addition to an operational amplifier, comparator latching output buffers and housekeeping logic. One counter is a clock counter which (after a reset pulse) starts counting clock pulses; when the required count is reached, the clock counter generates a pulse to start the end-of-conversion routine. The other counter is a data counter, which is reset synchronously with the clock counter and counts the number of times the I_{REF} current is switched into the summing input of the amplifier during the period defined by the clock counter.

When the Initiate Conversion input is strobed with a positive signal, the busy line latches high and a 10µs (times given are approximate) start up cycle begins. The integrating capacitor is discharged and both counters are reset during this start up period. Conversion begins at the end of the reset pulse and ends with a pulse generated either by the clock counter or by an overflow condition in the data counter. This pulse disables further inputs into both counters and triggers a 10µs shutdown cycle. During the shutdown cycle Data Valid goes low for 5µs. This binary sequence is shown in the timing diagrams. Busy is true high, and when the circuit is busy, Initiate Conversion has no effect and may be high or low. Data Valid is also true high. The data from a conversion remain valid for as long as power is applied to the circuit or until Data Valid falls at the end of a subsequent conversion, at which time the output data are updated to reflect the latest conversion.

Timing Diagrams (Rise, fall times = 200ns typ., C_L = 50pF)



Pin Functions

Initiate Conversion Input — Accepts CMOS and most 5V logic inputs. Applying a logic "1" to the Initiate Conversion pin initiates the A/D conversion cycle. Once conversion has been initiated, the cycle cannot be interrupted, and the Initiate Conversion pin is disabled until conversion is complete. Two modes of operation are permitted, clocked or free-running. For clocked operation the Initiate Conversion input is held at logic "0" for standby and taken to logic "1" when a conversion is desired. For free-running operation the Initiate Conversion pin is connected to V_{DD} or similar permanent logic "1" voltage.

Busy Output — A digital status output which is compatible with CMOS logic and low power TTL (can sink and source 500μA). A logic "1" output on the Busy pin indicates a conversion cycle is in process. A logic "1" to logic "0" transition indicates that conversion is complete and the result has been latched at the Digits Out pins. A logic "0" to logic "1" transition indicates a new conversion cycle has been initiated. If the device is operating in the free-running mode, the Busy output will remain low for approximately 2.5μs, marking the completion and initiation of consecutive conversion cycles.

Data Valid Output — A digital status which is compatible with CMOS logic and low power TTL (can sink and source 500μA). A logic "1" output at the Data Valid pin indicates that the Digits Out pins are latched with the result of the last conversion cycle. The Data Valid output goes to logic "0" approximately 5μs before the completion of a conversion cycle. During this 5μs interval new data is being transferred to the Digits Out pins, and the Digits Out are not valid.

Digits Out (Bit 0, Bit 1, etc.) — The binary digit outputs which are the result of the A/D conversion. These outputs are CMOS logic and low power TTL compatible.

Applications Information

Input/Output Relationships — The analog input voltage (V_{IN}) is related to the output by the transfer equation:

$$\text{DIGITAL COUNTS} = \frac{V_{IN} \cdot A \cdot R_{REF}}{R_{IN} \cdot V_{REF}}$$

A = 528 for 8700
A = 2064 for 8701
A = 8208 for 8702

where DIGITAL COUNTS is the value of the binary output word presented at Digits Out pins in response to V_{IN}.

The digital output code format is as follows:

ANALOG INPUT	DIGITAL OUTPUT
	MSB LSB
$V_{IN} \geq$ Full Scale	1 ...111... 1
= Full Scale − 1 LSB	1 ...111... 1
= 1 LSB	0 ...000... 1
≤ 0	0 ...000... 0

Two's complement coding can be generated by inverting the Most Significant Bit (MSB) signal.

External Component Selection — Obtaining a high accuracy conversion system depends on the voltage regulation of V_{REF} and the thermal stability of R_{IN} and R_{REF}. The exact dependence is given by the transfer function. System accuracy also depends, to a lesser degree, on the voltage regulation of V_{DD} and V_{SS}. The supply connections V_{DD} and V_{SS} should have bypass capacitors of value 0.1μF or larger right at the device pins.

R_{IN}, R_{REF} — Values of these components are chosen to give a full scale input current of approximately 10μA and a reference current of approximately −20μA.

$$R_{IN} \cong \frac{V_{IN\ FULL\ SCALE}}{10\mu A} \qquad R_{REF} \cong \frac{V_{REF}}{-20\mu A}$$

Examples:

$$R_{IN} \cong \frac{10V}{10\mu A} = 1M\Omega \qquad R_{REF} \cong \frac{-6.4V}{-20\mu A} = 320K\Omega$$

Note that these values are approximations, and the exact relationships are defined by the transfer equation. In practice, the value of R_{IN} typically would be trimmed using the optional gain adjust circuit to obtain full scale output at $V_{IN\ FULL\ SCALE}$ (see adjustment procedure.) Metal film resistors with 1% tolerance or better are recommended for high accuracy applications because of their thermal stability and low noise generation.

R_{BIAS} — Specifications for the 8700 series are based on $R_{BIAS} = 100K\Omega \pm 10\%$ unless otherwise noted. However, there are instances when the designer may want to change this resistor in order to affect the conversion time and the supply current. By decreasing R_{BIAS} the A/D will convert much faster and the supply current will be higher. (For example: When R_{BIAS} is 20K the conversion time is reduced by 1/3, and the supply current will increase from 2mA to 7mA.) Likewise, if the R_{BIAS} is increased the conversion time will be longer and the supply current will be much lower. (For example: When $R_{BIAS} = 1m\Omega$ the conversion time will be six times longer, and the supply current is now reduced to .5 mA.) For details of this relationship refer to AN-9 typical performance curves.

Applications Information (contd.)

R_{DAMP}– Exact value not critical but should have a nominal value of 100Ω ±10%. Locate close to pin 14.

C_{DAMP} – Exact value not critical but should have a nominal value of 270 pF ±20%. Locate close to pin 14.

C_{INT} – Exact value not critical but should have a nominal value of 68 pF ±10%. Low leakage types are recommended, although mica or ceramic devices can be used in applications where their temperature limits are not exceeded. Locate as close as possible to pins 14, 15.

V_{REF} – A negative reference voltage must be supplied. This may be obtained from a constant current source circuit or from the negative supply.

V_{DD}, V_{SS} – Power supplies of ±5V are recommended, with 1μF aluminum decoupling capacitors.

Adjustment Procedure – The test circuit diagram shows optional circuits for trimming the zero location and full scale gain. Because the digital outputs remain constant outside of the normal operating range (i.e. below zero and above full scale), it is recommended that transition points be used in setting the zero and full scale values. Recommended procedure is as follows:

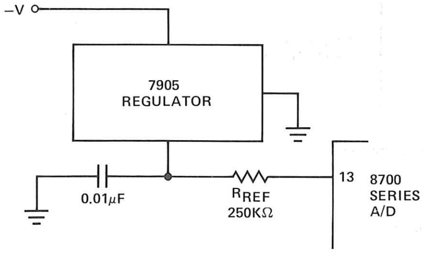
1. Set the initiate conversion control high to provide free-run operation and verify that converter is operating.
2. Set V_{IN} to +½ LSB and trim the zero adjust circuit to obtain a 000 . . . 000 . . . to 000 . . . 001 transition. This will correctly locate the zero end.
3. For full scale adjustment, set V_{IN} to the full scale value less 1½ LSB and trim the gain adjust circuit for a 111 . . . 110 to 111 . . . 111 transition.

If adjustments are performed in this order, there should be no interaction and they should not have to be repeated.

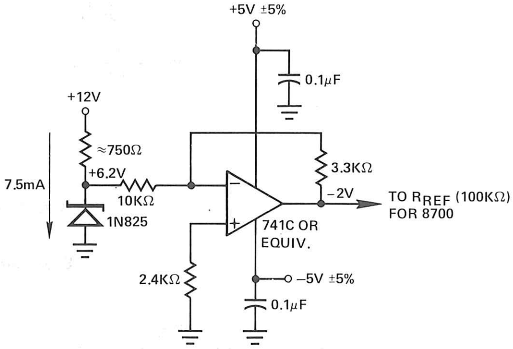
Typical Circuits

Reference Voltage Supply

A. –5V Reference



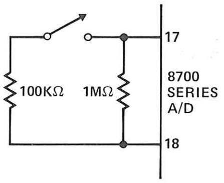
B. –2V Reference for 8700 using voltages derived from 8080A μP.



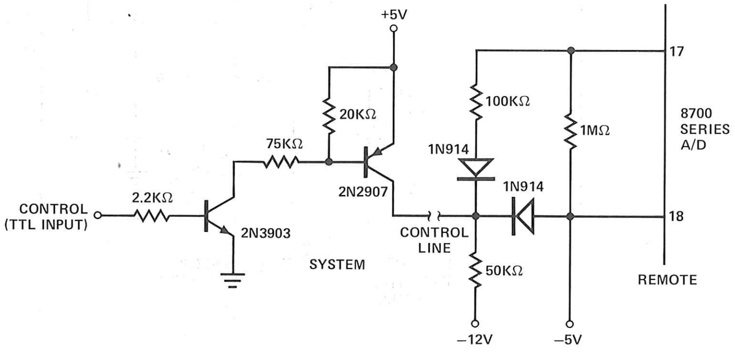
Power Reduction

Reduces power consumption to approximately 500μA.

A. Switch Controlled–relay could be substituted for switch.

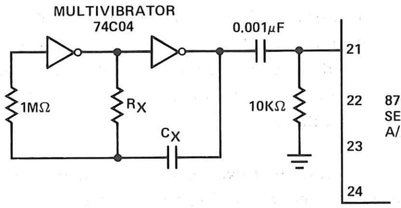


B. TTL System-Controlled–trades off additional power consumption at system for reduced usage at remote A/D.



Typical Circuits (contd.)

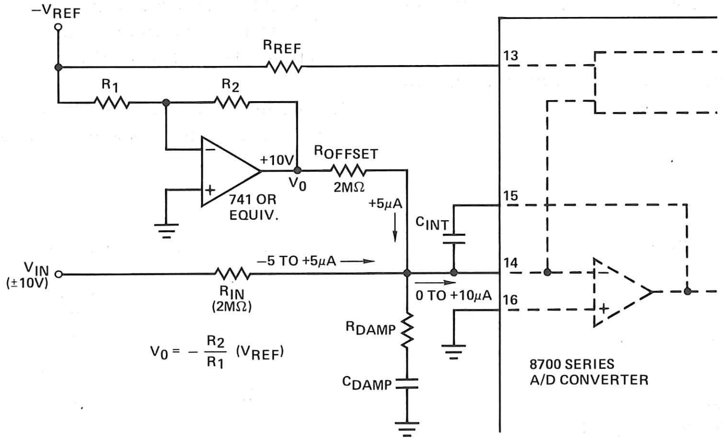
Free-Running Conversion Rate Control



Multivibrator circuit at Pin 21 (Initiate Conversion) strobes converter at rates slower than the normal free-run mode. ($\tau = R_X C_X$)

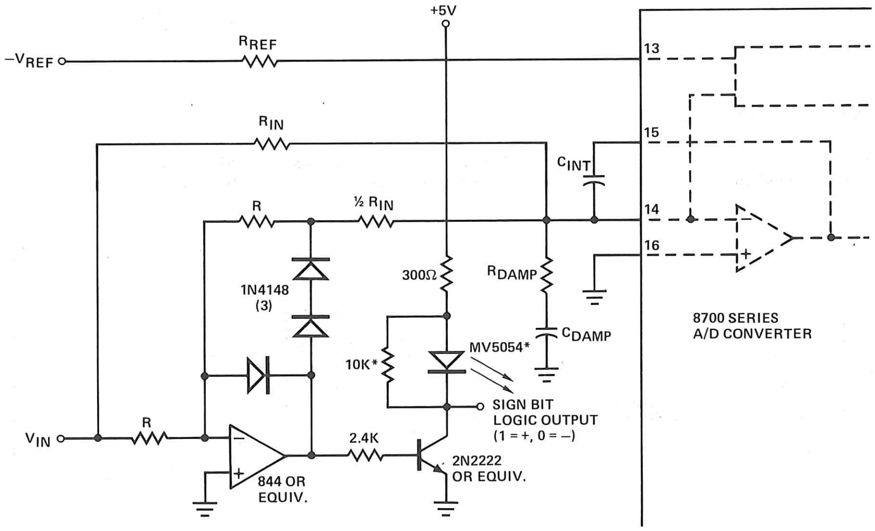
Bipolar Operation

A. Offset Binary



Two's complement coding may be generated by inverting the MSB output.

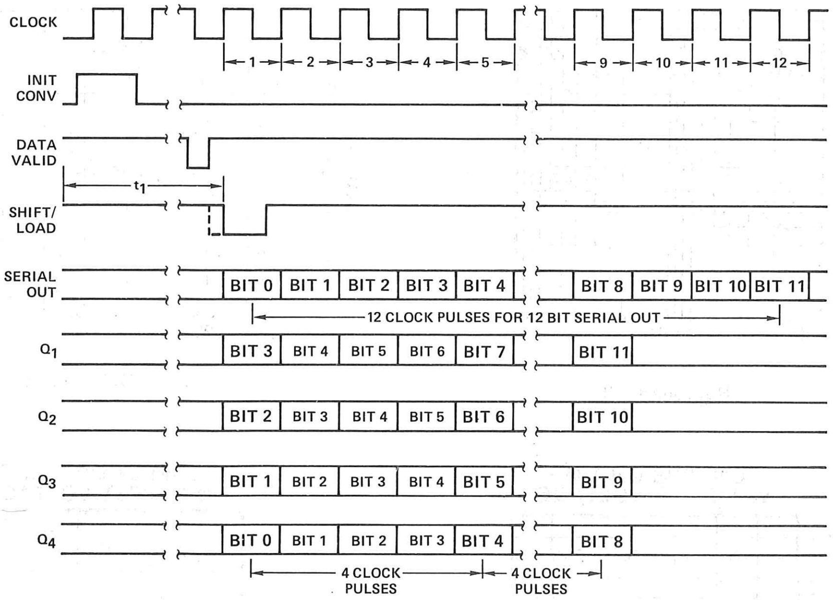
B. Magnitude-and-Sign Binary



*Optional visual indication of negative input

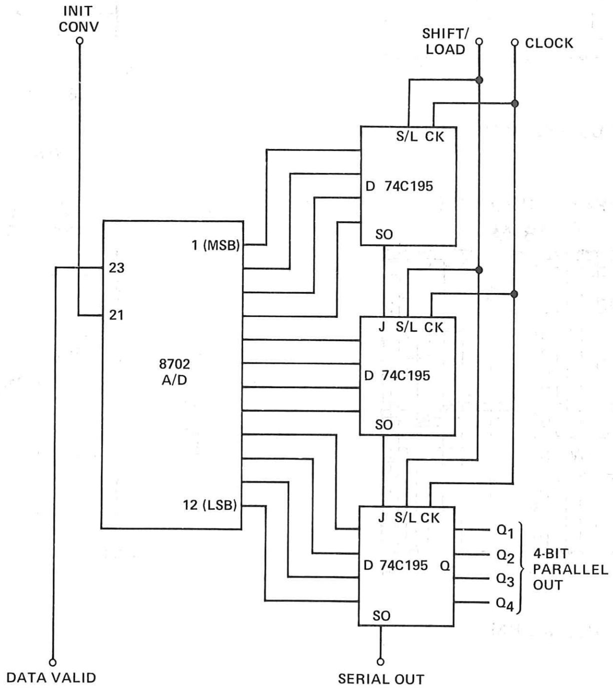
Typical Circuits (contd.)

12-Bit Serial or 3 x 4-Bit Parallel Output Format



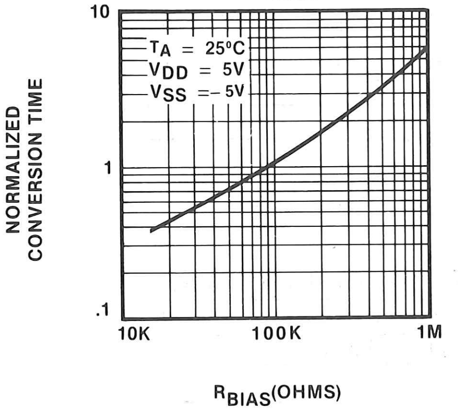
System reads parallel outputs at clock pulse 1, 5, 9

Shift/load may be taken low when Data Valid goes high or at fixed time t_1, after INIT CONV ($t_1 \geqslant 24$ ms for 8702). Shift/load then must return high before clock pulse 2 and must remain high until all data is read out. Recommended clock frequency 1 kHz min for serial, 750 Hz min for parallel output.

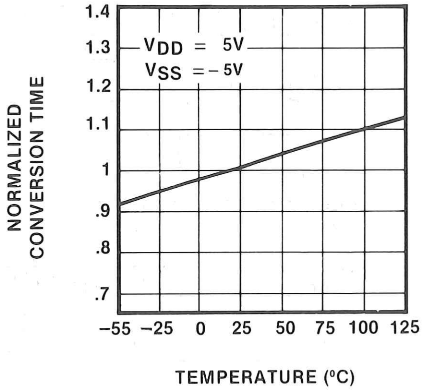


TYPICAL PERFORMANCE CURVES

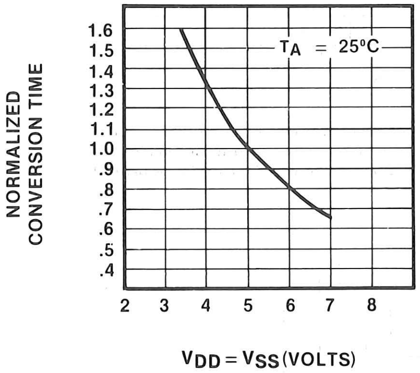
CONVERSION TIME vs R_{BIAS}



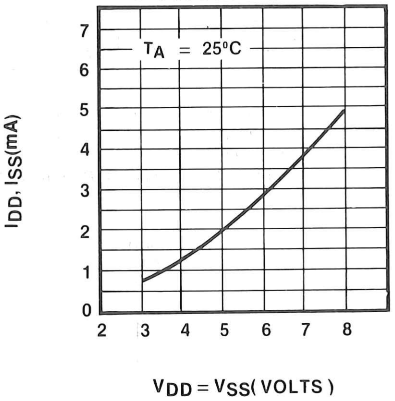
CONVERSION TIME vs TEMPERATURE



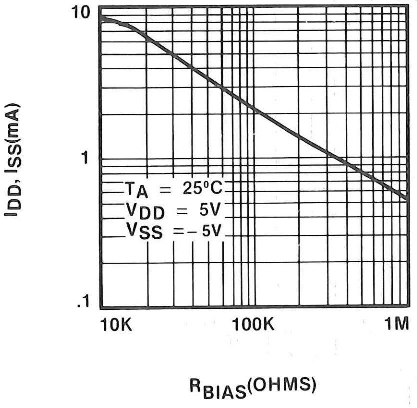
CONVERSION TIME vs SUPPLY VOLTAGE



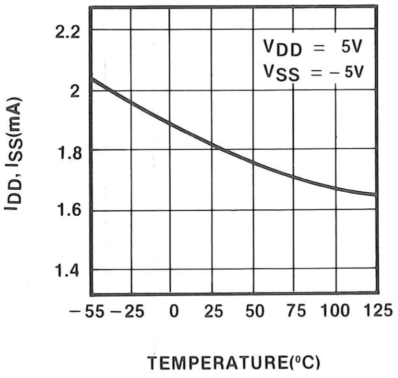
SUPPLY CURRENT vs SUPPLY VOLTAGE



SUPPLY CURRENT vs R_{BIAS}

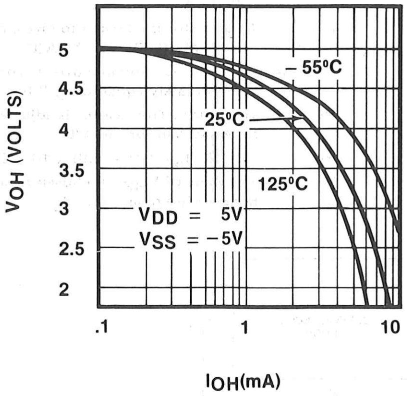


SUPPLY CURRENT vs TEMPERATURE

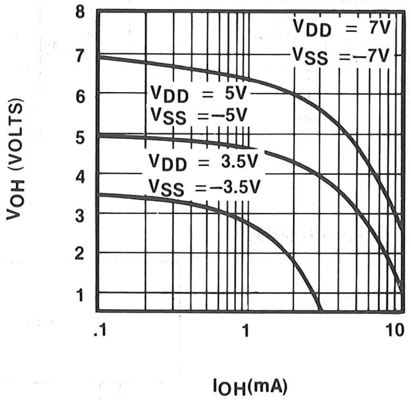


TYPICAL PERFORMANCE CURVES

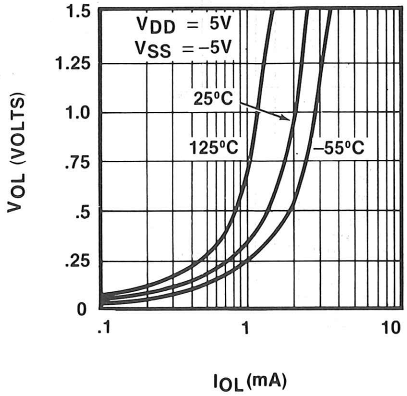
OUTPUT SOURCE CURRENT vs TEMPERATURE



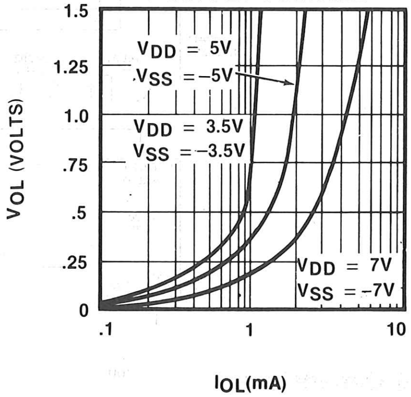
OUTPUT SOURCE CURRENT vs SUPPLY VOLTAGE



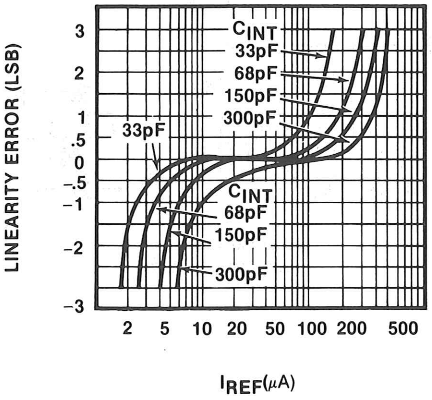
OUTPUT SINK CURRENT vs TEMPERATURE



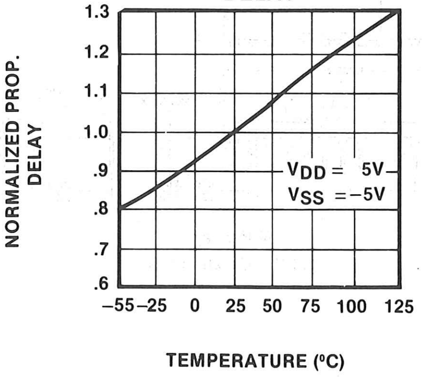
OUTPUT SINK CURRENT vs SUPPLY VOLTAGE



LINEARITY vs IREF

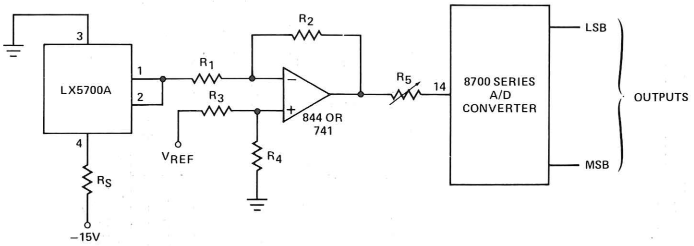


TRI-STATE PROPAGATION DELAY



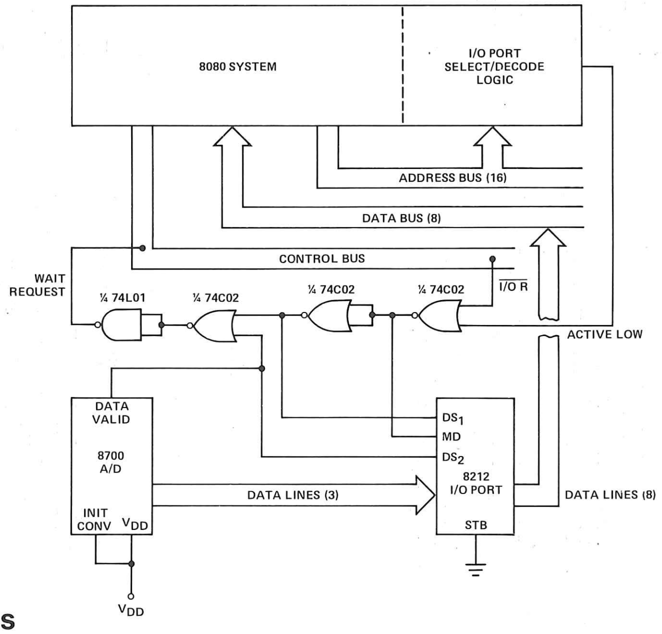
Typical Circuits (contd.)

Digital Temperature Monitor

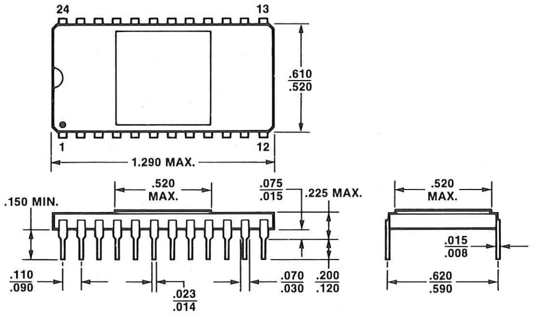


R_1.	Typically 10K min. This resistor should be chosen for the proper loading R_L of the LX5700A.
R_2.	This resistor is adjusted to give a full scale reading of 10.00V for the A/D.
$R3 = R4$.	Is set to give minimum offset. The value is approximately equal to $R_2 \parallel R_1$.
R_5.	1M typical. This resistor is adjusted to give full scale gain for the A/D.
R_S.	$7.5K\Omega$. $R_S = (V^+ - 6.8) \times 10^{-3}\Omega$.
V_{REF}.	The value of V_{REF} is chosen to set the temperature range desired.

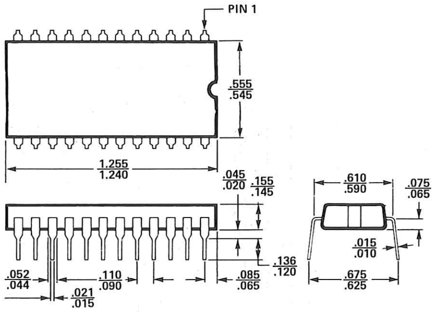
8-Bit Microprocessor Interface



Physical Dimensions



N Package
24-Pin Ceramic DIP



J Package
24-Pin Plastic DIP

Monolithic CMOS A/D Converters
8700 Series

8703, 8704, 8705
8, 10, 12-Bit
Three-State Binary

Features

Microprocessor Compatible

High Accuracy — Up to 12 Bit Resolution with < ±½ LSB Error

Monotonic Performance — No Missing Codes

Monolithic CMOS Construction Gives Low Power Dissipation — 20mW Typical

Contains All Required Active Elements — Needs Only Passive Support Components, Reference Voltage And Dual Power Supply

High Stability Over Full Temperature Range
- Gain Temperature Coefficient Typically <25ppm/°C
- Zero Drift Typically <30μV/°C
- Differential Non-Linearity Drift Typically <2.5ppm/°C

Latched Parallel Binary Outputs — Bus Organized

LPTTL And CMOS Compatible Outputs And Control Inputs

Strobed Or Free Running Conversion

Infinite Input Range — Any Positive Voltage Can Be Applied Via A Scaling Resistor

Absolute Maximum Ratings

Storage Temp.		− 65°C to + 150°C
Operating Temp.	BH/BN	− 55°C to + 125°C
	CN	− 40°C to + 85°C
	CJ	0°C to + 70°C
$V_{DD} - V_{SS}$		18V
I_{IN}		± 10mA
I_{REF}		± 10mA
Digital Input Voltage		− 0.3 to V_{DD} + 0.3V
Operating V_{DD} and V_{SS} Range		**3.5V to 7V**
Package Dissipation		500mW
Lead Temperature (Soldering, 10 seconds)		300°C

HANDLING PRECAUTIONS

The 8700 series are CMOS devices and must be handled correctly to prevent damage. Package and store only in conductive foam, anti-static tubes or other conductive material. Use proper anti-static handling procedures. Do not connect in circuits under "power on" conditions, as high transients may cause permanent damage.

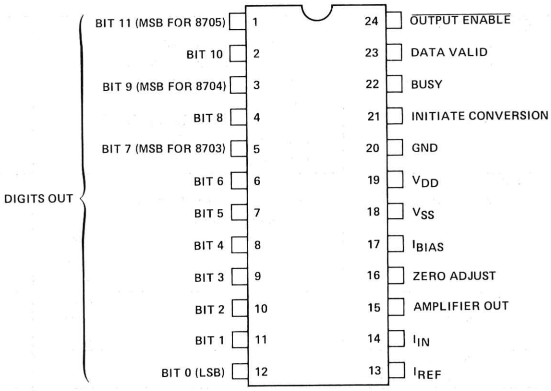
General Description

The Teledyne Semiconductor 8703/8704/8705 are 8/10/12 bit monolithic CMOS analog-to-digital converters. Fully self-contained in a single 24-pin dual in-line package, each converter requires only passive support components, voltage or current reference and power supplies.

Conversion is performed by an incremental charge balancing technique which has inherently high accuracy, linearity and noise immunity. An amplifier integrates the sum of the unknown analog current and pulses of a reference current, and the number of pulses (charge increments) needed to maintain the amplifier summing junction near zero is counted. At the end of conversion the total count is latched into the digital outputs as an 8/10/12 bit binary word. The $\overline{\text{OUTPUT ENABLE}}$ control switches the outputs to a high impedance or off state when held high. The off state allows bus organized output connections.

Connection Diagram

Order Part Numbers: See Page 2-20



Note: Pin 1 indicated by adjacent dot or indent (N package), end notch (J package), or lead extension (H package). Do not make connections to pin 1, 2, 3, or 4 on 8703; pin 1 or 2 on 8704. These pins are internally connected.

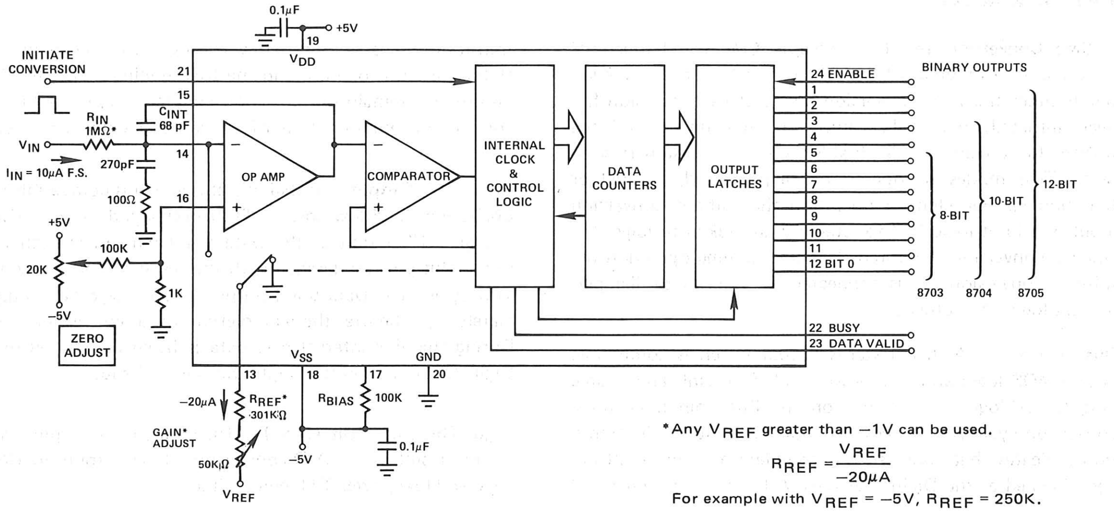
Electrical Characteristics

Unless otherwise specified, V_{DD} = +5V, V_{SS} = −5V, V_{GND} = 0, V_{REF} = −6.4V, R_{BIAS} = 100KΩ, test circuit shown. T_A = 25°C unless Full Temp. Range is specified. (−55°C to +125°C for BN and BH package, −40°C to +85°C for CN package, 0° to 70°C for CJ package.)

Parameter	Definition	Min	Typ	CJ/CN Max	BN/BH Max	Units	Conditions
Accuracy							
Resolution Accuracy	Binary word length of digital output						
	8703	8				Bits	
	8704	10				Bits	
	8705	12				Bits	
Relative Accuracy	Output deviation from straight line between normalized zero and full		± ¼	± ½	± ½	LSB	
	scale input 8705 CJ(only)		1.0	± 1.5		LSB	
Differential Non-Linearity	Deviation from 1LSB between transition points		± ¼	± ½	± ½	LSB	
Differential Non-Linearity Temperature Drift	Variation in Differential Non-Linearity due to temperature change		± 2.5	± 5	± 5	ppm/°C	Full Temp. Range
Gain Variance	Variation from exact A (compensate by trimming R_{IN} or R_{REF}		± 2	± 5	± 5	% of Nominal	
Gain Temperature Drift	Variation in A due to temperature change		± 25	± 75	± 80	ppm/°C	Full Temp. Range
Zero Offset	Correction at zero adjust to give zero output when input is zero		± 10	± 50	± 50	mV	I_{IN} = 0
Zero Temperature Drift	Variation in zero offset due to temperature change		± 3	± 5	± 8	ppm/°C	Full Temp. Range
Analog Inputs							
I_{IN} Full Scale	Full scale analog input current to achieve specified accuracy		10			µA	
I_{REF} (Note 1)	Reference current input to achieve specified accuracy		−20			µA	
Digital Inputs							
V_{IN} (1)	Logical "1" input threshold for $\overline{\text{Output Enable}}$ and Initiate Conversion Input	3.5				V	Full Temp. Range
V_{IN} (0)	Logical "0" input threshold for $\overline{\text{Output Enable}}$ and Initiate Conversion Input			1.5	1.5	V	Full Temp. Range
Propagation Delay							
Output Enable	T_{PLH}, T_{PHL}		500		1,000	ns	C_L = 100 pF, R_L = 1KΩ
Digital Outputs							
$I_{0(OFF)}$	Off-state output current		0.1	± 10	± 10	µA	$\overline{OE}$ = 3.5V, O.4V < V_c < 2.4
V_{OUT} (1)	Logical "1" output voltage for						Full Temp. Range
	Digits Out, Busy, and Data	4.5				V	I_{OUT} = −10µA
	Valid Outputs	2.4				V	I_{OUT} = −500µA
V_{OUT} (0)	Logical "0" output voltage for Digits Out, Busy, and Data Valid Outputs			0.4	0.4	V	Full Temp. Range V_{DD} = 4.75V, I_{OUT} = 500µA
Dynamic							
Conversion Time	Time required to perform one complete A/D conversion						
	8703		1.25	1.8	1.8	ms	Full Temp. Range
	8704		5	6	6	ms	
	8705		20	24	24	ms	
Conversion Rate in Free-Run Mode	8703	555	800			Conv'ns per Second	$V_{INIT\ CONV}$ = +5V
	8704	167	200				
	8705	42	50				
Minimum Pulse Width for Initiate Conversion		500				ns	Full Temp. Range
Supply Current							
I_{DD} Quiescent	Current required from positive supply during operation						
(H/N Package)			1.4	2.5	3.5	mA	Full Temp. Range
(J Package)			1.4	5.0		mA	$V_{INIT\ CONV}$ = OV
I_{SS} Quiescent	Current required from negative supply during operation						
(H/N Package)			−1.6	−2.5	−3.5	mA	Full Temp. Range
(J Package)			−1.6	−5.0		mA	$V_{INIT\ CONV}$ = OV
Supply Sensitivity	Change in full scale gain vs supply voltage change		± 0.5	± 1.0	± 1.0	%/V	V_{DD} ± 1V, V_{SS} ± 1V
	Change in full scale gain vs supply voltage change for tracking supplies.		± 0.05	± 0.1	± 0.1	%/V	$\lvert V_{DD}\rvert = \lvert V_{SS}\rvert$ = 5V ± 1V

NOTE: I_{IN} and I_{REF} pins connect to the summing junction of an operational amplifier. Voltage sources cannot be attached directly but must be buffered by external resistors. See Test **Circuit.**

Test Circuit



*Any V_{REF} greater than −1V can be used.

$$R_{REF} = \frac{V_{REF}}{-20\mu A}$$

For example with $V_{REF} = -5V$, $R_{REF} = 250K$.

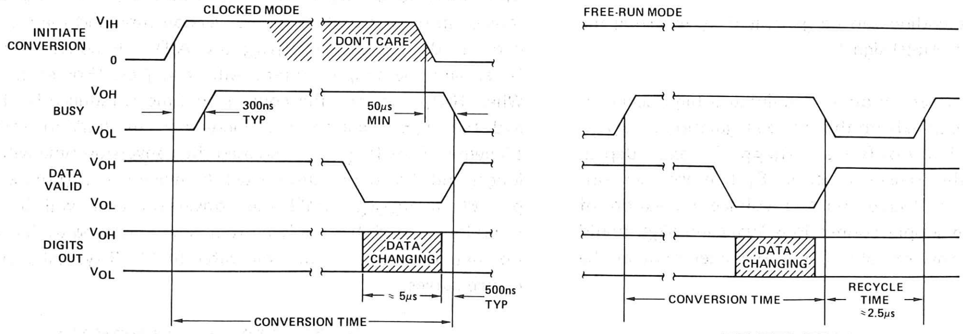
Circuit Description

During conversion the sum of a continuous current I_{IN} and pulses of a reference current I_{REF} is integrated for a fixed number of clock periods. I_{IN} is proportional to the analog input voltage; I_{REF} is proportional to the reference voltage and is of opposite sign to I_{IN}. I_{REF} is switched in for exactly one clock period just frequently enough to maintain the summing input of the integrator near zero. Thus, the charge from the continuous I_{IN} current is balanced against the pulses of I_{REF} current. The total number of I_{REF} pulses needed during the conversion period to maintain the charge balance is counted, and the result (in binary) is latched into the outputs at the end of conversion.

The converter contains two counters and a clock in addition to an operational amplifier, comparator, latching output buffers and housekeeping logic. One counter is a clock counter which (after a reset pulse) starts counting clock pulses; when the required count is reached, the clock counter generates a pulse to start the end-of-conversion routine. The other counter is a data counter, which is reset synchronously with the clock counter and counts the number of times the I_{REF} current is switched into the summing input of the amplifier during the period defined by the clock counter.

When the Initiate Conversion input is strobed with a positive signal, the busy line latches high and a 10μs (times given are approximate) start up cycle begins. The integrating capacitor is discharged and both counters are reset during this start up period. Conversion begins at the end of the reset pulse and ends with a pulse generated either by the clock counter or by an overflow condition in the data counter. This pulse disables further inputs into both counters and triggers a 10μs shutdown cycle. During the shutdown cycle Data Valid goes low for 5μs. This binary sequence is shown in the timing diagrams. Busy is true high, and when the circuit is busy, Initiate Conversion has no effect and may be high or low. Data Valid is also true high. The data from a conversion remain valid for as long as power is applied to the circuit or until Data Valid falls at the end of a subsequent conversion, at which time the output data are updated to reflect the latest conversion.

Timing Diagrams (Rise, fall times = 200ns typ., C_L = 50pF)



Pin Functions

Initiate Conversion Input — Accepts CMOS and most 5V logic inputs. Applying a logic "1" to the Initiate Conversion pin initiates the A/D conversion cycle. Once conversion has been initiated, the cycle cannot be interrupted, and the Initiate Conversion pin is disabled until conversion is complete. Two modes of operation are permitted, clocked or free-running. For clocked operation the Initiate Conversion input is held at logic "0" for standby and taken to logic "1" when a conversion is desired. For free-running operation the Initiate Conversion pin is connected to V_{DD} or similar permanent logic "1" voltage.

Busy Output — A digital status output which is compatible with CMOS logic and low power TTL (can sink and source 500μA). A logic "1" output on the Busy pin indicates a conversion cycle is in process. A logic "1" to logic "0" transition indicates that conversion is complete and the result has been latched at the Digits Out pins. A logic "0" to logic "1" transition indicates a new conversion cycle has been initiated. If the device is operating in the free-running mode, the Busy output will remain low for approximately 2.5μs, marking the completion and initiation of consecutive conversion cycles.

Data Valid Output — A digital status which is compatible with CMOS logic and low power TTL (can sink and source 500μA). A logic "1" output at the Data Valid pin indicates that the Digits Out pins are latched with the result of the last conversion cycle. The Data Valid output goes to logic "0" approximately 5μs before the completion of a conversion cycle. During this 5μs interval new data is being transferred to the Digits Out pins, and the Digits Out are not valid.

Digits Out (Bit 0, Bit 1, etc.) — The binary digit outputs which are the result of the A/D conversion. These outputs are CMOS logic and low power TTL compatible.

Applications Information

Input/Output Relationships — The analog input voltage (V_{IN}) is related to the output by the transfer equation:

$$\text{DIGITAL COUNTS} = \frac{V_{IN} \cdot A \cdot R_{REF}}{R_{IN} \cdot V_{REF}}$$

A = 528 for 8703
A = 2064 for 8704
A = 8208 for 8705

where DIGITAL COUNTS is the value of the binary output word presented at Digits Out pins in response to V_{IN}.

The digital output code format is as follows:

ANALOG INPUT	DIGITAL MSB	LSB
$V_{IN} \geq$ Full Scale	1 . . . 1 1 1 . . . 1	
= Full Scale — 1 LSB	1 . . . 1 1 1 . . . 1	
= 1 LSB	0 . . . 0 0 0 . . . 1	
≤ 0	0 . . . 0 0 0 . . . 0	

Two's complement coding can be generated by inverting the Most Significant Bit (MSB) signal.

External Component Selection — Obtaining a high accuracy conversion system depends on the voltage regulation of V_{REF} and the thermal stability of R_{IN} and R_{REF}. The exact dependence is given by the transfer function. System accuracy also depends, to a lesser degree, on the voltage regulation of V_{DD} and V_{SS}. The supply connections V_{DD} and V_{SS} should have bypass capacitors of value 0.1μF or larger right at the device pins.

R_{IN}, R_{REF} — Values of these components are chosen to give a full scale input current of approximately 10μA and a reference current of approximately —20μA.

$$R_{IN} \cong \frac{V_{IN\ FULL\ SCALE}}{10\mu A} \qquad R_{REF} \cong \frac{V_{REF}}{-20\mu A}$$

Examples:

$$R_{IN} \cong \frac{10V}{10\mu A} = 1M\Omega \qquad R_{REF} \cong \frac{-6.4V}{-20\mu A} = 320K\Omega$$

Note that these values are approximations, and the exact relationships are defined by the transfer equation. In practice, the value of R_{IN} typically would be trimmed using the optional gain adjust circuit to obtain full scale output at $V_{IN\ FULL\ SCALE}$ (see adjustment procedure.) Metal film resistors with 1% tolerance or better are recommended for high accuracy applications because of their thermal stability and low noise generation.

R_{BIAS} — Specifications for the 8700 series are based on R_{BIAS} = 100KΩ ± 10% unless otherwise noted. However, there are instances when the designer may want to change this resistor in order to affect the conversion time and the supply current. By decreasing R_{BIAS} the A/D will convert much faster and the supply current will be higher. (For example: When R_{BIAS} is 20K the conversion time is reduced by 1/3, and the supply current will increase from 2mA to 7mA.) Likewise, if the R_{BIAS} is increased the conversion time will be longer and the supply current will be much lower. (For example: When R_{BIAS} = 1mΩ the conversion time will be six times longer, and the supply current is now reduced to .5 mA.) For details of this relationship refer to AN-9 typical performance curves.

Applications Information (contd.)

R_{DAMP}– Exact value not critical but should have a nominal value of 100Ω ±10%. Locate close to pin 14.

C_{DAMP} – Exact value not critical but should have a nominal value of 270 pF ±20%. Locate close to pin 14.

C_{INT} – Exact value not critical but should have a nominal value of 68 pF ±10%. Low leakage types are recommended, although mica or ceramic devices can be used in applications where their temperature limits are not exceeded. Locate as close as possible to pins 14, 15.

V_{REF} – A negative reference voltage must be supplied. This may be obtained from a constant current source circuit or from the negative supply.

V_{DD}, V_{SS} – Power supplies of ±5V are recommended, with 0.1μF decoupling capacitors.

Adjustment Procedure – The test circuit diagram shows optional circuits for trimming the zero location and full scale gain. Because the digital outputs remain constant outside of the normal operating range (i.e. below zero and above full scale), it is recommended that transition points be used in setting the zero and full scale values. Recommended procedure is as follows:

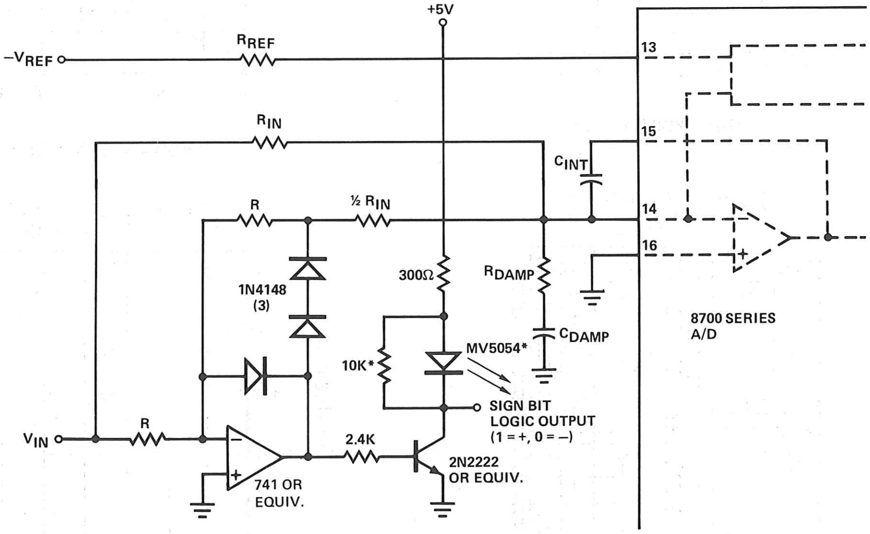
1. Set the initiate conversion control high to provide free-run operation and verify that converter is operating.
2. Set V_{IN} to +½ LSB and trim the zero adjust circuit to obtain a 000 . . . 000 . . . to 000 . . . 001 transition. This will correctly locate the zero end.
3. For full scale adjustment, set V_{IN} to the full scale value less 1½ LSB and trim the gain adjust circuit for a 111 . . . 110 to 111 . . . 111 transition.

If adjustments are performed in this order, there should be no interaction and they should not have to be repeated.

Application/Design Circuits

Bipolar Operation (+ and – inputs)

Absolute Value Circuit with Sign

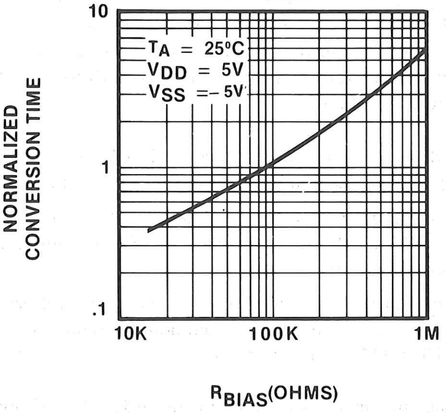


*Optional visual indication of negative input

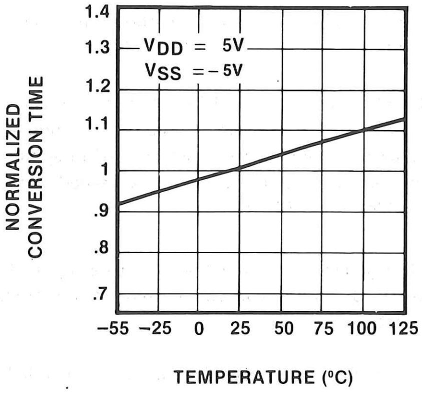
NOTE: Values for R should be between 10KΩ and 100KΩ

TYPICAL PERFORMANCE CURVES

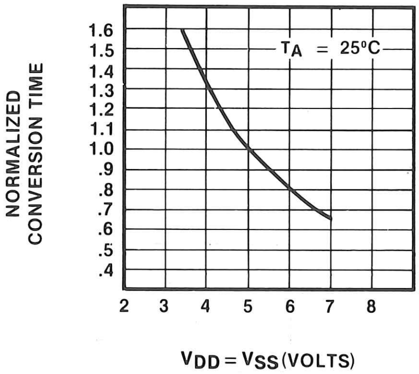
CONVERSION TIME
vs R_{BIAS}



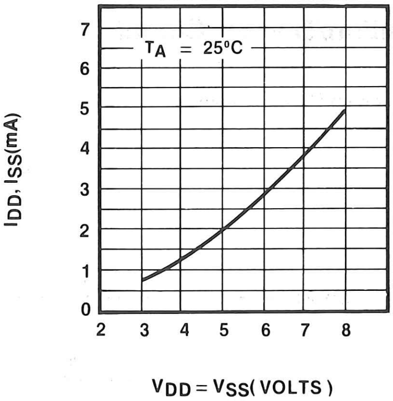
CONVERSION TIME
vs TEMPERATURE



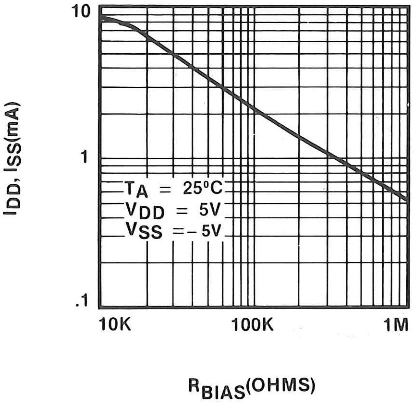
CONVERSION TIME
vs SUPPLY VOLTAGE



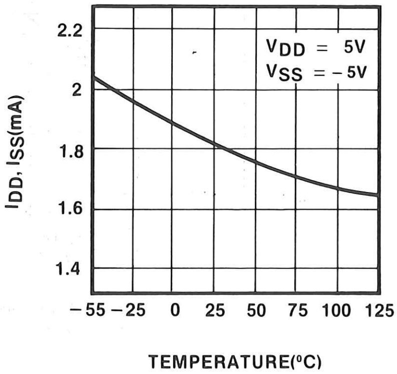
SUPPLY CURRENT
vs SUPPLY VOLTAGE



SUPPLY CURRENT
vs R_{BIAS}

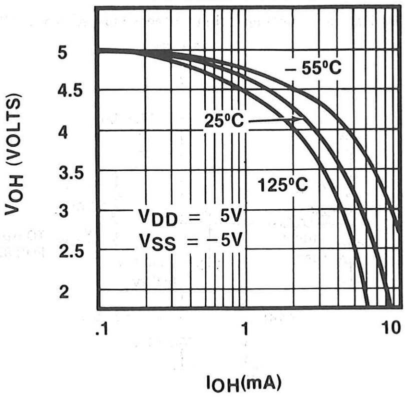


SUPPLY CURRENT
vs TEMPERATURE

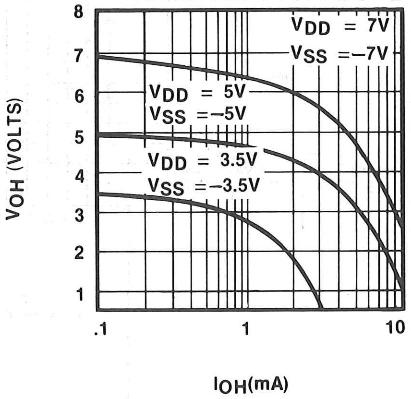


TYPICAL PERFORMANCE CURVES

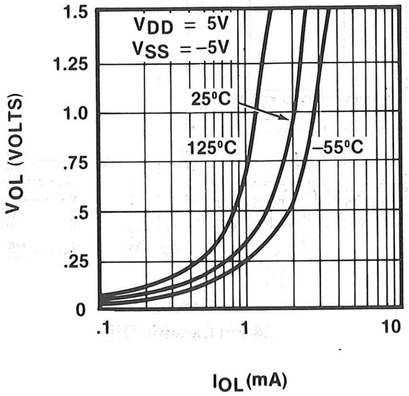
OUTPUT SOURCE CURRENT vs TEMPERATURE



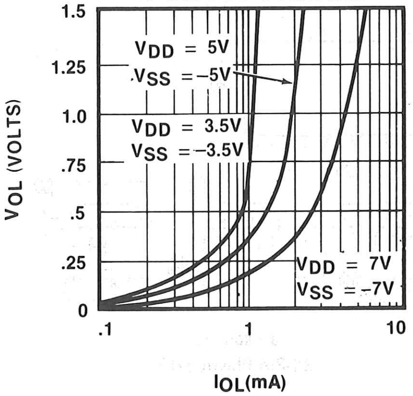
OUTPUT SOURCE CURRENT vs SUPPLY VOLTAGE



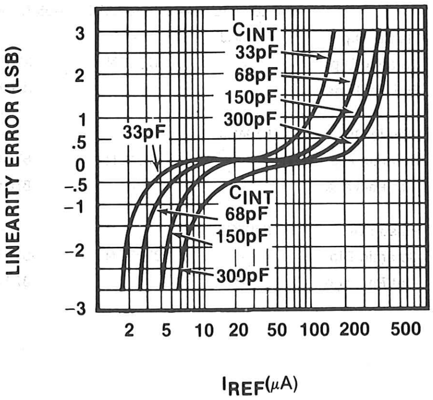
OUTPUT SINK CURRENT vs TEMPERATURE



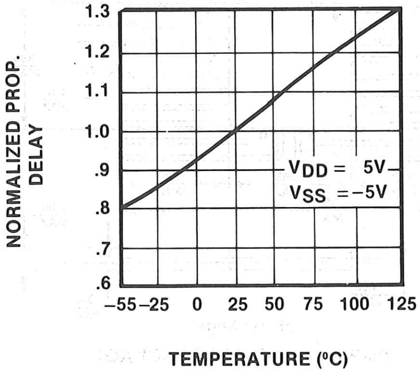
OUTPUT SINK CURRENT vs SUPPLY VOLTAGE



LINEARITY vs IREF

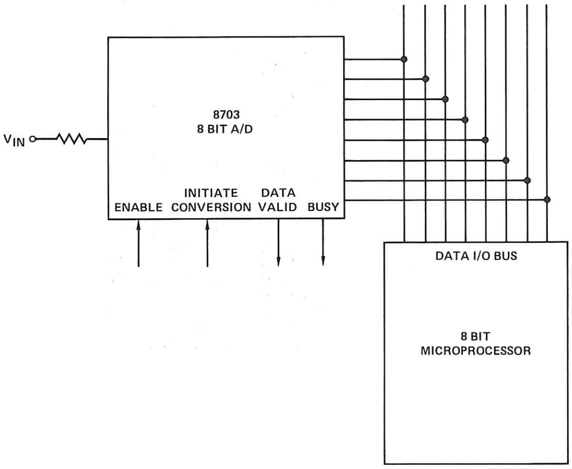


TRI-STATE PROPAGATION DELAY



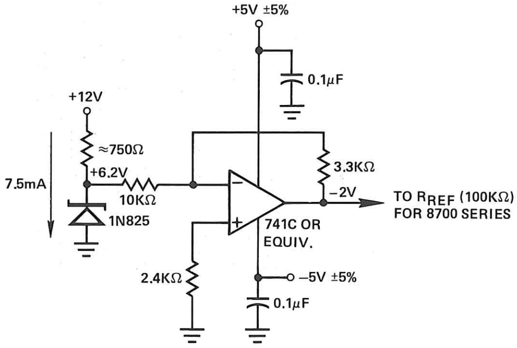
Application/Design Circuits (contd.)

8-Bit Microprocessor Interface

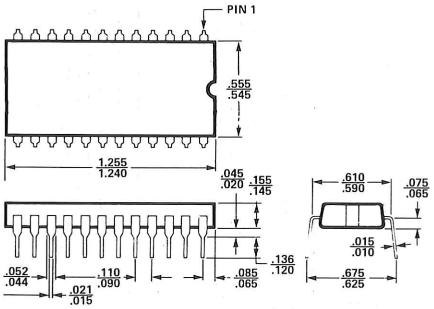


Reference Voltage Supply

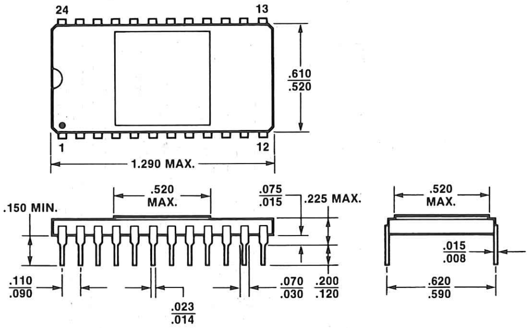
2V Reference voltage using voltages derived from 8080A μP.



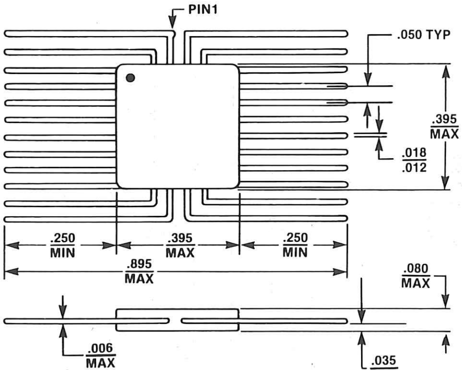
Physical Dimensions



J Package
24-Pin Plastic DIP



N Package
24-Pin Ceramic DIP



H Package
24-Pin Ceramic FLAT PACKAGE

Order Part Numbers:

		0 to 70°C	−40 to +85°C	−55 to +125°C
8 BIT	Plastic Dip	8703CJ	-	-
	Ceramic Dip	-	8703CN	8703BN
	Flat Package	-	-	8703BH
10 BIT	Plastic Dip	8704CJ	-	-
	Ceramic Dip	-	8704CN	8704BN
	Flat Package	-	-	8704BH
12 BIT	Plastic Dip	8705CJ	-	-
	Ceramic Dip	-	8705CN	8705BN
	Flat Package	-	-	8705BH

Monolithic CMOS A/D Converters

8700 Series

8750

3½ Digit

Features

High Accuracy — 3½ Digit Resolution with <±0.025% Error

Monotonic Performance — No Missing Codes

Monolithic CMOS Construction Gives Low Power Dissipation — 20mW Typical

Contains All Required Active Elements — Needs Only Passive Support Components, Reference Voltage And Dual Power Supply

High Stability Over Full Temperature Range
- Gain Temperature Coefficient Typically <25ppm/°C
- Zero Drift Typically <30μV/°C
- Differential Non-Linearity Drift Typically <2.5ppm/°C

Latched Parallel BCD Outputs

LPTTL And CMOS Compatible Outputs And Control Inputs

Strobed Or Free Running Conversion

Infinite Input Range — Any Positive Voltage Can Be Applied Via A Scaling Resistor

Absolute Maximum Ratings

Storage Temp.		−65°C to +150°C
Operating Temp.	BH/BN	−55°C to +125°C
	CN	−40°C to +85°C
	CJ	0°C to +70°C
$V_{DD} - V_{SS}$		18V
I_{IN}		±10mA
I_{REF}		±10mA
Digital Input Voltage		−0.3 to V_{DD} +0.3V
Operating V_{DD} and V_{SS} Range		**3.5V to 7V**
Package Dissipation		500mW
Lead Temperature (Soldering, 10 seconds)		300°C

HANDLING PRECAUTIONS

The 8700 series are CMOS devices and must be handled correctly to prevent damage. Package and store only in conductive foam, anti-static tubes or other conductive material. Use proper anti-static handling procedures. Do not connect in circuits under "power on" conditions, as high transients may cause permanent damage.

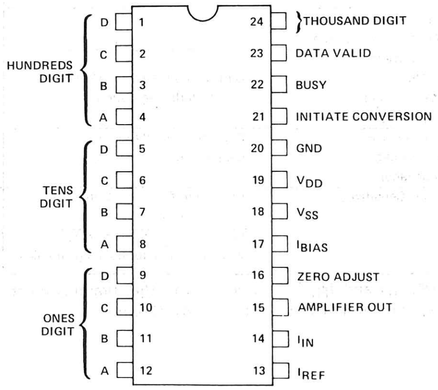
General Description

The Teledyne Semiconductor 8750 is a 3 ½ digit monolithic CMOS analog-to-digital converter. Fully self-contained in a single 24-pin dual in-line package, the converter requires only passive support components, voltage or current reference and power supplies.

Conversion is performed by an incremental charge balancing technique which has inherently high accuracy, linearity and noise immunity. An amplifier integrates the sum of the unknown analog current and pulses of a reference current, and the number of pulses (charge increments) needed to maintain the amplifier summing junction near zero is counted. At the end of conversion the total count is latched into the digital outputs in a 3 ½ digit BCD digital format.

Connection Diagram

Order Part Numbers: See Page 2-28



NOTE: Pin 1 indicated by adjacent dot or indent (N package), or end notch (J package),lead extension (H package).

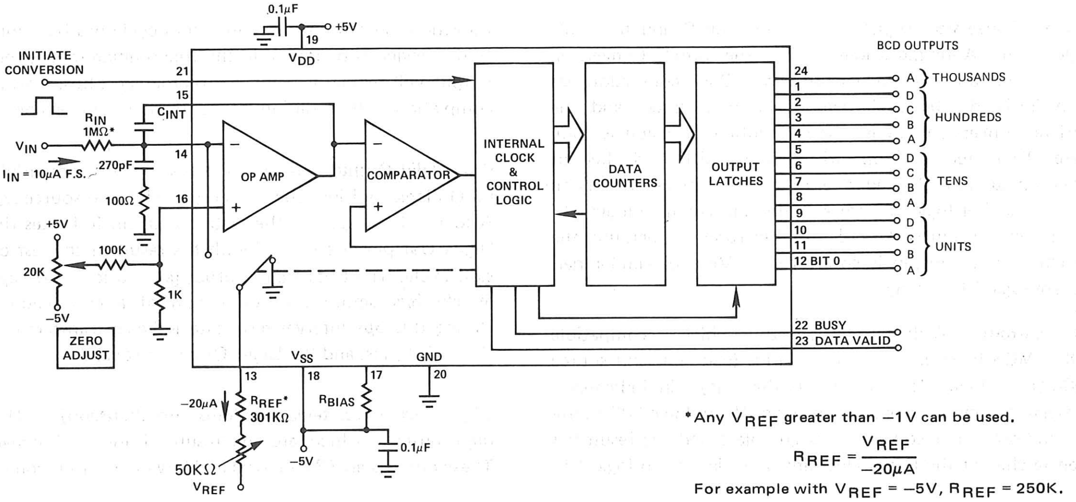
Electrical Characteristics

Unless otherwise specified, V_{DD} = +5V, V_{SS} = –5V, V_{GND} = 0, V_{REF} = –6.4V, R_{BIAS} = 100KΩ, test circuit shown. T_A = 25°C unless Full Temp. Range is specified. (–55°C to +125°C for BN and BH package, –40°C to +85°C for CM package, 0° to 70°C for CJ package.)

				CJ/CN	BN/BH		
Parameter	**Definition**	**Min**	**Typ**	**Max**	**Max**	**Units**	**Conditions**
Accuracy							
Resolution Accuracy	BCD word length of digital output	3 1/2 (1999 counts)				Digits	
Relative Accuracy	Output deviation from straight line between normalized zero and full scale input			0.025	0.025	%	
Differential Non-Linearity	Deviation from 1LSB between transition points			0.025	0.025	%	
Differential Non-Linearity Temperature Drift	Variation in Differential Non-Linearity due to temperature change		± 2.5	± 5	± 5	ppm/°C	Full Temp. Range
Gain Variance	Variation from exact A (compensate sate by trimming R_{IN} or R_{REF})		± 2	± 5	± 5	% of Nominal	
Gain Temperature Drift	Variation in A due to temperature change		± 25	± 75	± 80	ppm/°C	Full Temp. Range
Zero Offset	Correction at zero adjust to give zero output when input is zero		± 10	± 50	± 50	mV	I_{IN} = 0
Zero Temperature Drift	Variation in zero offset due to temperature change		± 3	± 5	± 8	ppm/°C	Full Temp. Range
Analog Inputs							
I_{IN} Full Scale	Full scale analog input current to achieve specified accuracy		10			μA	
I_{REF} (Note 1)	Reference current input to achieve specified accuracy		–20			μA	
Digital Inputs							
V_{IN} (1)	Logical "1" input threshold for Initiate Conversion Input	3.5				V	Full Temp. Range
V_{IN} (0)	Logical "0" input threshold for Initiate Conversion Input			1.5	1.5	V	Full Temp. Range
Digital Outputs							
V_{OUT} (1)	Logical "1" output voltage for Digits Out, Busy, and Data Valid Outputs	4.5 2.4				V V	Full Temp. Range I_{OUT} = –10μA I_{OUT} = –500μA
V_{OUT} (0)	Logical "0" output voltage for Digits Out, Busy, and Data Valid Outputs			0.4	0.4	V	Full Temp. Range V_{DD} = 4.75V I_{OUT} = 500μA
Dynamic							
Conversion Time	Time required to perform one complete A/D conversion		10	12	12	ms	Full Temp. Range
Conversion Rate in Free-Run Mode		84	100			Conv'ns per Second	$V_{INIT\ CONV}$ = +5V
Minimum Pulse Width for Initiate Conversion		500				ns	Full Temp. Range
Supply Current							
I_{DD} Quiescent	Current required from positive supply during operation						Full Temp. Range $V_{INIT\ CONV}$ = OV
(H/N Package)			1.4	2.5	3.5	mA	
(J Package)			1.4	5.0		mA	
I_{SS} Quiescent	Current required from negative supply during operation						Full Temp. Range $V_{INIT\ CONV}$ = OV
(H/N Package)			– 1.6	–2.5	– 3.5	mA	
(J Package)			– 1.6	– 5.0		mA	
Supply Sensitivity	Change in full scale gain vs supply voltage change		± 0.5	± 1.0	± 1.0	%/V	V_{DD} ± 1V, V_{SS} ± 1.V
	Change in full scale gain vs supply voltage change for tracking supplies		± 0.05	± 0.1	± 0.1	%/V	$\lvert V_{DD}\rvert = \lvert V_{SS}\rvert$ = 5V ± 1V

NOTE: I_{IN} and I_{REF} pins connect to the summing junction of an operational amplifier. Voltage sources cannot be attached directly but must be buffered by external resistors. See Test Circuit.

Test Circuit



*Any V_{REF} greater than $-1V$ can be used.

$$R_{REF} = \frac{V_{REF}}{-20\mu A}$$

For example with $V_{REF} = -5V$, $R_{REF} = 250K$.

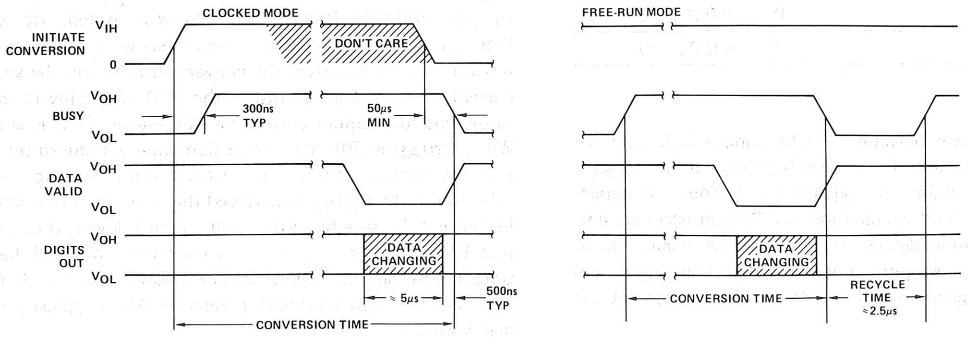
Circuit Description

During conversion the sum of a continuous current I_{IN} and pulses of a reference current I_{REF} is integrated for a fixed number of clock periods. I_{IN} is proportional to the analog input voltage; I_{REF} is proportional to the reference voltage and is of opposite sign to I_{IN}. I_{REF} is switched in for exactly one clock period just frequently enough to maintain the summing input of the integrator near zero. Thus, the charge from the continuous I_{IN} current is balanced against the pulses of I_{REF} current. The total number of I_{REF} pulses needed during the conversion period to maintain the charge balance is counted, and the result (in BCD) is latched into the outputs at the end of conversion.

The converter contains two counters and a clock in addition to an operational amplifier, comparator, latching output buffers and housekeeping logic. One counter is a clock counter which (after a reset pulse) starts counting clock pulses; when the required count is reached, the clock counter generates a pulse to start the end-of-conversion routine. The other counter is a data counter, which is reset synchronously with the clock counter and counts the number of times the I_{REF} current is switched into the summing input of the amplifier during the period defined by the clock counter.

When the Initiate Conversion input is strobed with a positive signal, the busy line latches high and a 10μs (times given are approximate) start up cycle begins. The integrating capacitor is discharged and both counters are reset during this start up period. Conversion begins at the end of the reset pulse and ends with a pulse generated either by the clock counter or by an overflow condition in the data counter. This pulse disables further inputs into both counters and triggers a 10μs shutdown cycle. During the shutdown cycle Data Valid goes low for 5μs. This binary sequence is shown in the timing diagrams. Busy is true high, and when the circuit is busy, Initiate Conversion has no effect and may be high or low. Data Valid is also true high. The data from a conversion remain valid for as long as power is applied to the circuit or until Data Valid falls at the end of a subsequent conversion, at which time the output data are updated to reflect the latest conversion.

Timing Diagrams (Rise, fall times = 200ns typ., C_L = 50pF)



Pin Functions

Initiate Conversion Input – Accepts CMOS and most 5V logic inputs. Applying a logic "1" to the Initiate Conversion pin initiates the A/D conversion cycle. Once conversion has been initiated, the cycle cannot be interrupted, and the Initiate Conversion pin is disabled until conversion is complete. Two modes of operation are permitted, clocked or free-running. For clocked operation the Initiate Conversion input is held at logic "0" for standby and taken to logic "1" when a conversion is desired. For free-running operation the Initiate Conversion pin is connected to V_{DD} or similar permanent logic "1" voltage.

Busy Output -- A digital status output which is compatible with CMOS logic and low power TTL (can sink and source 500µA). A logic "1" output on the Busy pin indicates a conversion cycle is in process. A logic "1" to logic "0" transition indicates that conversion is complete and the result has been latched at the Digits Out pins. A logic "0" to logic "1" transition indicates a new conversion cycle has been initiated. If the device is operating in the free-running mode, the Busy output will remain low for approximately 2.5µs, marking the completion and initiation of consecutive conversion cycles.

Data Valid Output – A digital status which is compatible with CMOS logic and low power TTL (can sink and source 500µA). A logic "1" output at the Data Valid pin indicates that the Digits Out pins are latched with the result of the last conversion cycle. The Data Valid output goes to logic "0" approximately 5µs before the completion of a conversion cycle. During this 5µs interval new data is being transferred to the Digits Out pins, and the Digits Out are not valid.

Digits Out (ones, tens, hundreds and thousand) – The BCD digit outputs which are the result of the A/D conversion. These outputs are CMOS logic and low power TTL compatible.

Applications Information

Input/Output Relationships – The analog input voltage (V_{IN}) is related to the output by the transfer equation:

$$\text{DIGITAL COUNTS} = \frac{V_{IN} \cdot A \cdot R_{REF}}{R_{IN} \cdot V_{REF}}$$

$$A = 4128$$

where DIGITAL COUNTS is the value of the BCD output word presented at Digits Out pins in response to V_{IN}.

The digital output code format is as follows:

ANALOG INPUT	DIGITAL OUTPUT
$V_{IN} \geq$ Full Scale	1100110011001
= Full Scale – 1 LSB	1100110011001
= 1 LSB	0 . . . 0 0 0 . . . 1
≤ 0	0 . . . 0 0 0 . . . 0

External Component Selection – Obtaining a high accuracy conversion system depends on the voltage regulation of V_{REF} and the thermal stability of R_{IN} and R_{REF}. The exact dependence is given by the transfer function. System accuracy also depends, to a lesser degree, on the voltage regulation of V_{DD} and V_{SS}. The supply connections V_{DD} and V_{SS} should have bypass capacitors of value 0.1µF or larger right at the device pins.

R_{IN}, R_{REF} – Values of these components are chosen to give a full scale input current of approximately 10µA and a reference current of approximately –20µA.

$$R_{IN} \cong \frac{V_{IN}\ \text{FULL SCALE}}{10\mu A} \qquad R_{REF} \cong \frac{V_{REF}}{-20\mu A}$$

Examples:

$$R_{IN} \cong \frac{10V}{10\mu A} = 1M\Omega \qquad R_{REF} \cong \frac{-6.4V}{-20\mu A} = 320K\Omega$$

Note that these values are approximations, and the exact relationships are defined by the transfer equation. In practice, the value of R_{IN} typically would be trimmed using the optional gain adjust circuit to obtain full scale output at V_{IN} FULL SCALE (see adjustment procedure.) Metal film resistors with 1% tolerance or better are recommended for high accuracy applications because of their thermal stability and low noise generation.

R_{BIAS} – Specifications for the 8750 series are based on R_{BIAS} = 100KΩ ± 10% unless otherwise noted. However, there are instances when the designer may want to change this resistor in order to affect the conversion time and the supply current. By decreasing R_{BIAS} the A/D will convert much faster and the supply current will be higher. (For example: When R_{BIAS} is 20K the conversion time is reduced by 1/3, and the supply current will increase from 2mA to 7mA.) Likewise, if the R_{BIAS} is increased the conversion time will be longer and the supply current will be much lower. (For example: When R_{BIAS} = 1mΩ the conversion time will be six times longer, and the supply current is now reduced to .5 mA.) For details of this relationship refer to AN-9 typical performance curves.

Applications Information (contd.)

R_{DAMP}– Exact value not critical but should have a nominal value of 100Ω ±10%. Locate close to pin 14.

C_{DAMP} – Exact value not critical but should have a nominal value of 270 pF ±20%. Locate close to pin 14.

C_{INT} – Exact value not critical but should have a nominal value of 68 pF ±10%. Low leakage types are recommended, although mica or ceramic devices can be used in applications where their temperature limits are not exceeded. Locate as close as possible to pins 14, 15.

V_{REF} – A negative reference voltage must be supplied. This may be obtained from a constant current source circuit or from the negative supply.

V_{DD}, V_{SS} – Power supplies of ±5V are recommended, with 0.1μF decoupling capacitors.

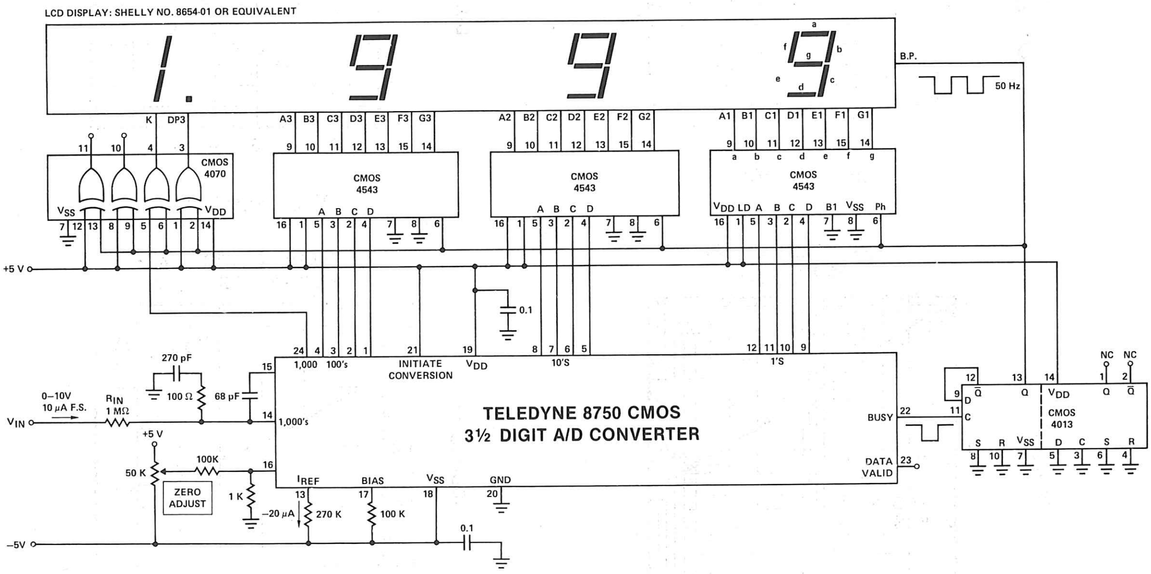
Adjustment Procedure – The test circuit diagram shows optional circuits for trimming the zero location and full scale gain. Because the digital outputs remain constant outside of the normal operating range (i.e. below zero and above full scale), it is recommended that transition points be used in setting the zero and full scale values. Recommended procedure is as follows:

1. Set the initiate conversion control high to provide free-run operation and verify that converter is operating.
2. Set V_{IN} to +½ LSB and trim the zero adjust circuit to obtain a 000 . . . $00\underline{0}$ . . . to 000 . . . $00\underline{1}$ transition. This will correctly locate the zero end.
3. For full scale adjustment, set V_{IN} to the full scale value less 1½ LSB and trim the gain adjust circuit for a $110011001100\underline{0}$ to 1100110011001 transition.

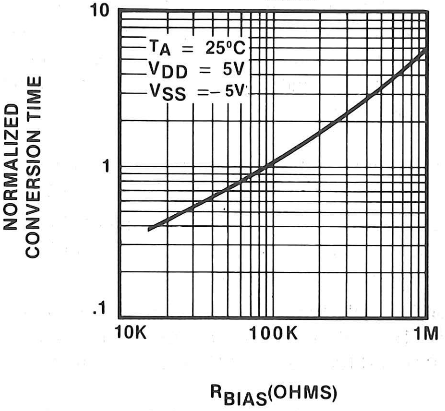
If adjustments are performed in this order, there should be no interaction and they should not have to be repeated.

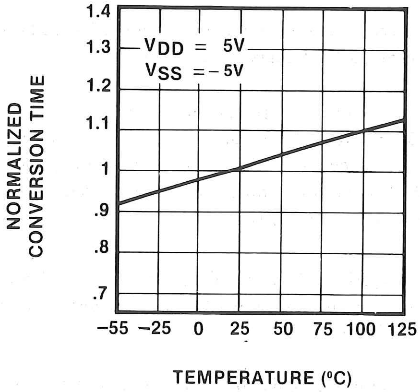
Application/Design Circuits

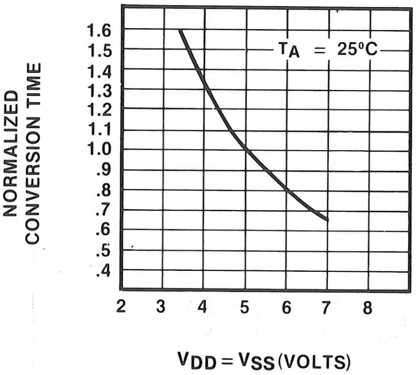
3½ Digit A/D with LCD Display

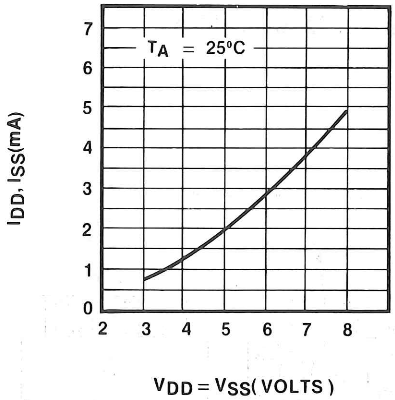


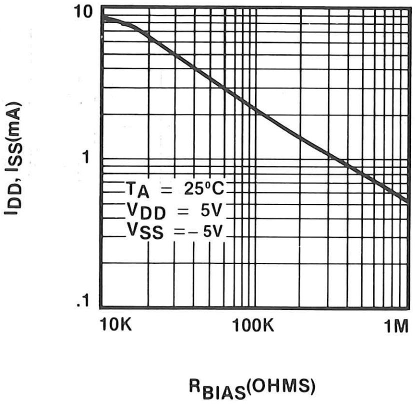
TYPICAL PERFORMANCE CURVES

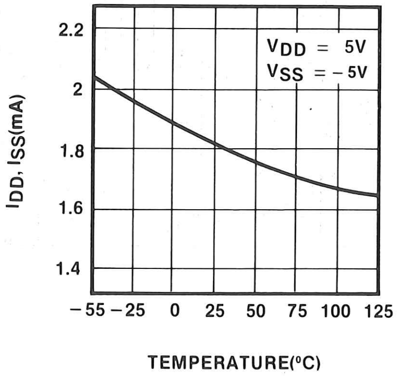

CONVERSION TIME vs R_{BIAS}


CONVERSION TIME vs TEMPERATURE


CONVERSION TIME vs SUPPLY VOLTAGE

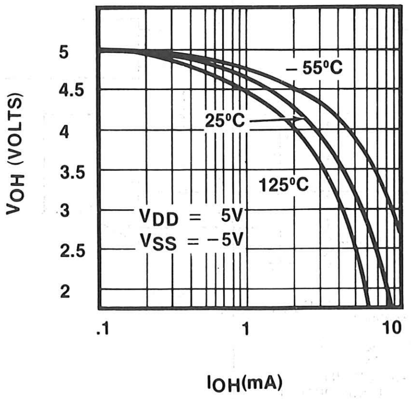

SUPPLY CURRENT vs SUPPLY VOLTAGE


SUPPLY CURRENT vs R_{BIAS}

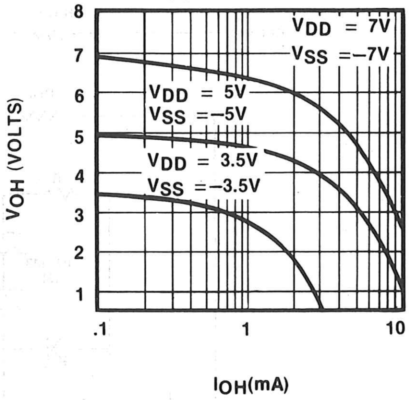

SUPPLY CURRENT vs TEMPERATURE

TYPICAL PERFORMANCE CURVES

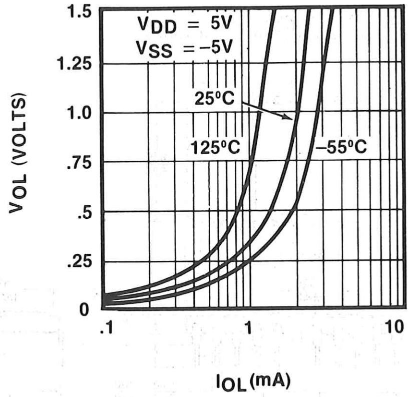
OUTPUT SOURCE CURRENT vs TEMPERATURE



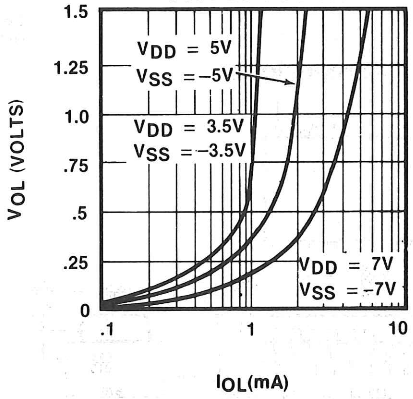
OUTPUT SOURCE CURRENT vs SUPPLY VOLTAGE



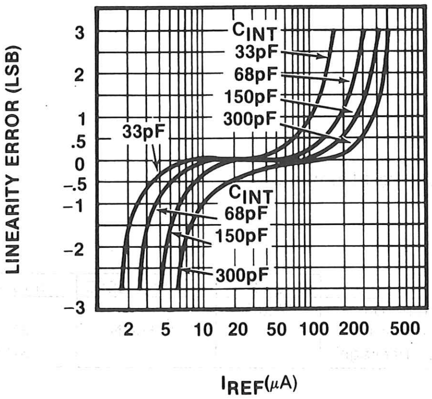
OUTPUT SINK CURRENT vs TEMPERATURE



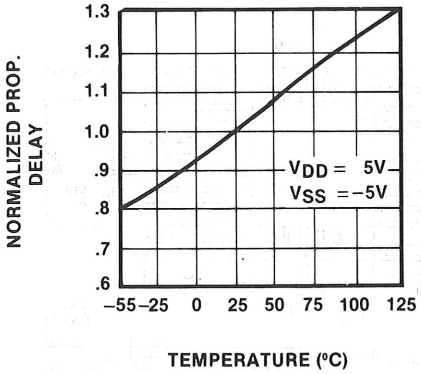
OUTPUT SINK CURRENT vs SUPPLY VOLTAGE



LINEARITY vs IREF



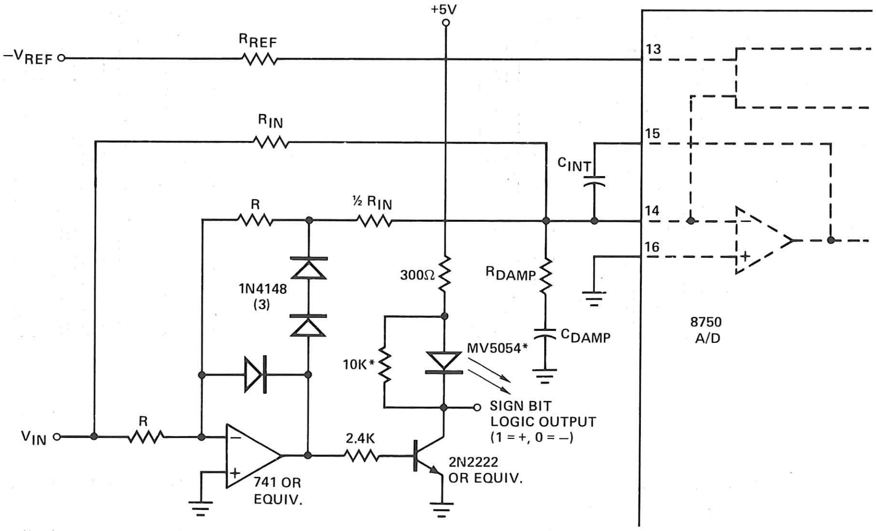
TRI-STATE PROPAGATION DELAY



Application/Design Circuits (contd.)

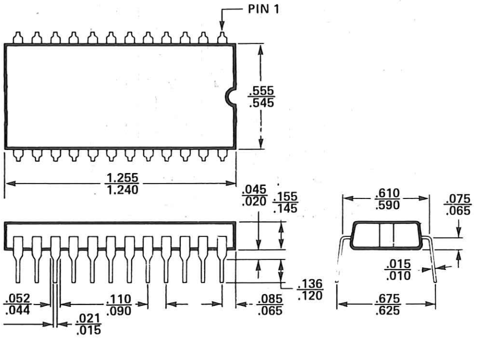
Bipolar Operation (+ and − inputs)

Absolute Value Circuit with Sign

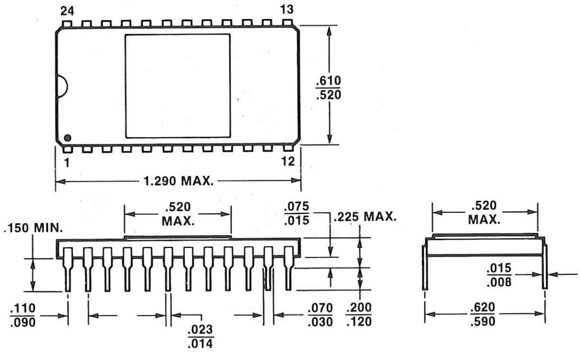


*Optional visual indication of negative input
NOTE: Values for R should be between 10KΩ and 100KΩ

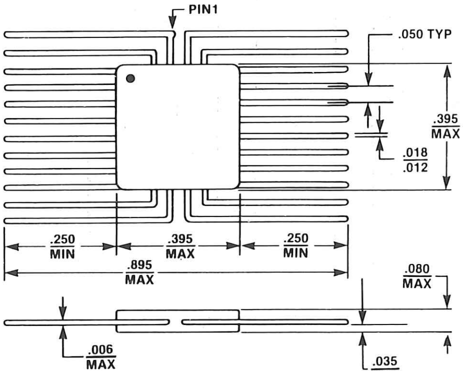
Physical Dimensions



J Package
24-Pin Plastic DIP



N Package
24-Pin Ceramic DIP



H Package
24-Pin Ceramic FLAT PACKAGE

Order Part Numbers:

	0 to 70°C	−40 to +85°C	−55 to +125°C
Plastic Dip	8750CJ	-	-
Ceramic Dip	-	8750CN	8750BN
Flat Package	-	-	8750BH

Monolithic CMOS A/D Converter
8700 Series

8751
3-1/2 Digit Multiplexed

Features

Auto-Zero, Auto-Polarity
BCD Output, TTL, CMOS Compatible
Display Hold Input
End of Conversion Signal
Two Input Ranges — 199.9mV and 1.999V
Low Input Current — 10pA, typical
Low Input Noise: 30μV typical
Low Power Consumption — 10mW, typical
Internal or External Clock

Applications

Digital Voltmeters
Bright LED Displays
Gas Discharge Displays
Microprocessor Interfacing
Data Printing and Recording

Ordering Information

28-Pin Plastic	28-Pin Ceramic
(-40°C to +85°C) 8751CJ	(-40°C to +85°C) 8751CN

General Description

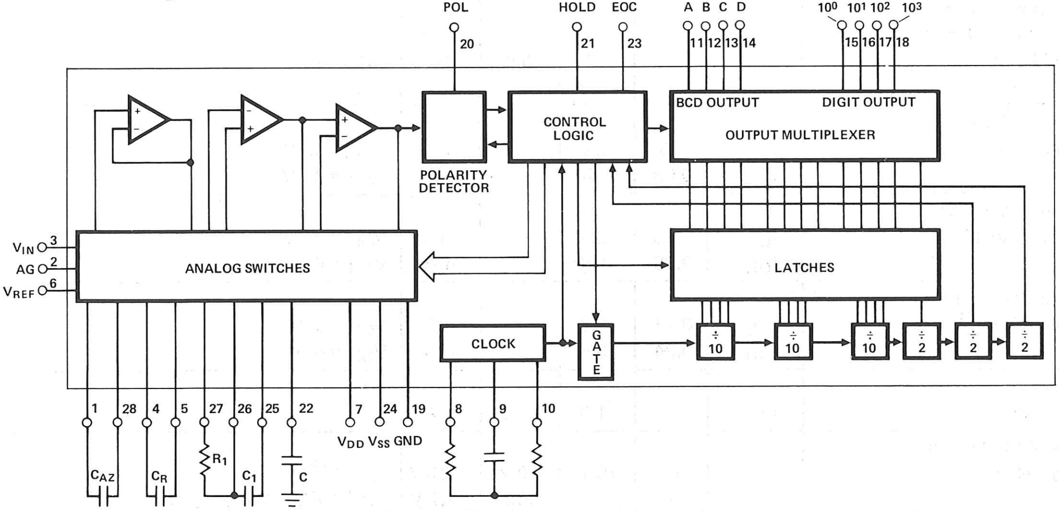
The 8751 is a 3½ digit monolithic CMOS A/D converter, designed for low power panel meter applications with a minimum of external components. Only four resistors and five capacitors are required to implement the A/D function.

The chip contains a dual-slope A/D converter and all digital circuitry necessary to provide a multiplexed BCD output. An external resistor and capacitor determine the internal clock frequency, allowing up to 15 conversions per second. Also, an internal network of analog switches provides a logic output for polarity (auto-polarity) and compensation for internal offsets (auto-zero) during each conversion cycle.

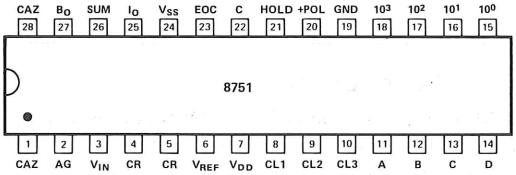
The display reading may be held at any time by applying a logic "0" to the Display Hold input. This has no effect on the conversion cycle. The display automatically blanks when the input voltage exceeds full scale (F/S) for the selected input range. This range is set by the reference voltage, ie. F/S = 1.999V for V_{REF} = 1.0V, and F/S = 199.9mV for V_{REF} = 0.1V.

The 8751 supply voltages may range from 4.5V to 6.0V positive and -2.5V to -8.0V negative with ±5.0V recommended. A 28 pin package is available in plastic or ceramic DIP. The 8751 is made with a CMOS process featuring high density logic with a double layer of metal interconnections.

Functional Diagram



Pin Configuration



Absolute Maximum Ratings

	Min.	Max.	Units
Storage Temperature	-65	+150	°C
Operating Temperature	-40	+85	°C
Power Dissipation			
CJ		1,200	mW
CN		1,200	mW
(Above 50°C derate by 12 mW/°C)			
Lead Temperature (Soldering, 10 seconds)		300	°C
Clock Frequency		60	kHz
V_{DD}–AG	-0.3	+6.5	V
V_{DD}–GND	-0.3	+6.5	V
GND–V_{SS}	-9.0	+0.3	V
AG–V_{SS}	-9.0	+0.3	V

Electrical Characteristics

Unless otherwise specified, V_{DD} = +5V, V_{SS} = -5V, Temperature range -40°C to +85°C, (R_1 = 1MΩ, C_1 = 0.1μF, V_R = +1V: F_{CLK} = 10 kHz at 2V F.S.) (R_1 = 100K, C_1 = 0.1μF, V_R = 0.1V at 200mV F.S.)

Characteristics	Symbol	Min.	Typ.	Max.	Units	Conditions
Accuracy		-0.05		+0.05	% Rdg	V_{REF} = 1.00V
		-1		+1	Count	V_{REF} = 1.00V
Stability				±0.5	LSD	V_{IN} = 1.99V, V_{REF} = 1V
				±1.0	LSD	V_{IN} = 199mV, V_{REF} = 0.1V, R_1 = 100K
Zero		-0.5		+0.5	LSD	T_A = 25°C, V_{IN} = 0V, V_{REF} = 1V
		-1.0		+1.0	LSD	-40°C ⩽ T_A ⩽ 85°C, V_{IN} = 0V, V_{REF} = 1V
Analog Input Bias Current			±10	±100	pA	T_A = 25°C
Reference Input Bias Current			±10	±100	pA	T_A = 25°C
Plus and Minus Full Scale Symmetry		-1.0		+1.0	LSD	V_{IN} = ±1.990V, V_{REF} = 1V
Output Voltage Pins 11 to 18 and 20						
"0" Level	V_{OL}	–	0	0.05	V	GND = 0V
"1" Level	V_{OH}	4.95	5.0	–	V	V_{DD} = 5.0V
Output Current Pins 11 to 14	I_{OL}	1.6	2.8		mA	V_{OL} = 0.4V
	I_{OH}	0.08	0.14		mA	V_{OH} = 4.6V
Output Current Pins 15 to 18	I_{OL}	0.28	0.50		mA	V_{OL} = 0.4V
	I_{OH}	0.28	0.50		mA	V_{OH} = 4.6V
Output Current Polarity, Pin 20	I_{OL}	0.17	0.3		mA	V_{OL} = 0.4V
	I_{OH}	0.34	0.6		mA	V_{OH} = 4.6V
Supply Current V_{DD} to V_{SS}	I_Q		1.0	1.5	mA	
Supply Rejection V_{DD} to V_{SS}		0	±0.1	±0.2	LSD/V	T_A = 25°C, V_{REF} = 1V
		0		±0.5	LSD/V	-40°C ⩽ T_A ⩽ +85°C, V_{REF} = 1V

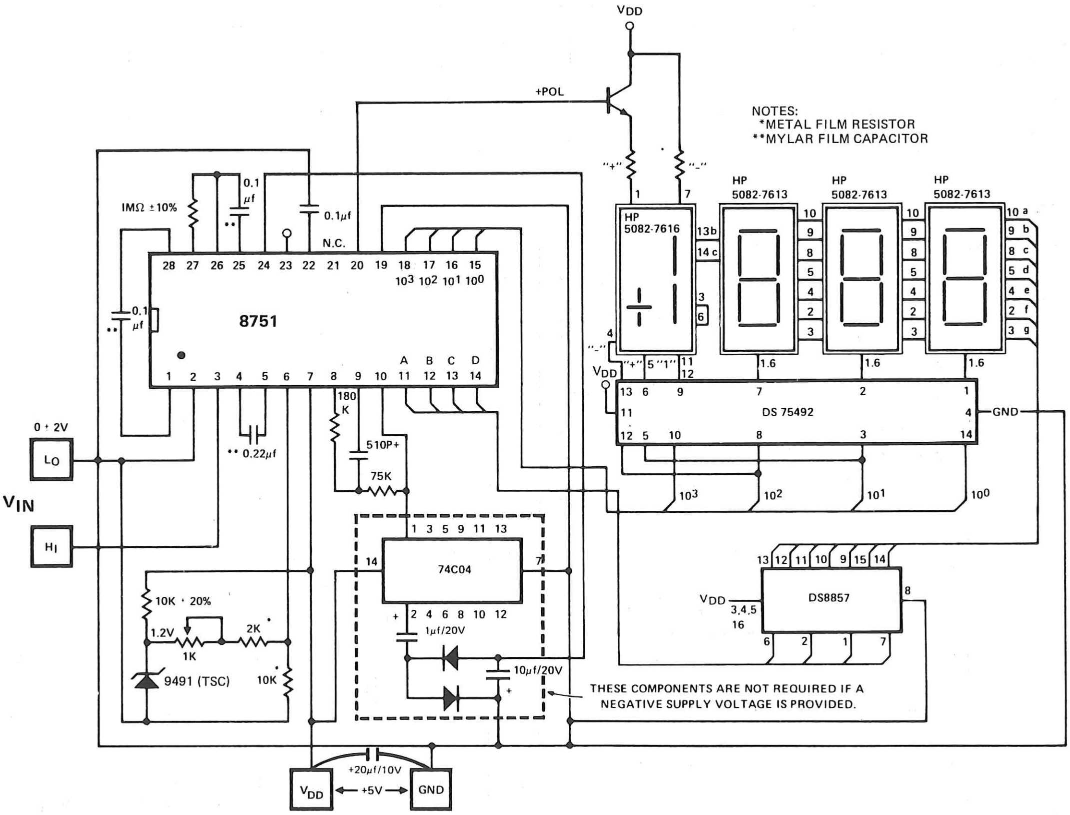
Recommended Operating Conditions

Parameter	Symbol	Value	Unit
V_{DD} to AG (Analog GND)	V_{DD}	+4.5 to 6.0	Vdc
V_{SS} to AG	V_{SS}	-2.5 to -8.0	Vdc
Clock Frequency	F_{CLK}	10 to 20	kHz

Pin Description

Pin	Mnemonic	Description
1	C_{AZ}	Auto-zero capacitor. Connect between pin 1 and pin 28. Use a low leakage mylar capacitor, with value according to input range: 0.47μF 199.9mV range 0.1μF 1.999V range
2	AG	Analog ground. This is the reference level for the unknown input voltage (V_{IN}) and reference voltage (V_R). Connect to digital ground, pin 19.
3	V_{IN}	Analog input voltage. Typical input current is 10 pA.
4	C_R	Connect between pin 4 and pin 5. The reference voltage stored on this capacitor provides an input of either polarity, depending on the state of internal switches. Mylar is recommended, and value depends on input range: 0.47μF 199.9mV range 0.22μF 1.999V range
5	C_R	See pin 4.
6	V_R	Reference voltage input. Value is 0.1V for 199.9mV range, or 1.0V for 1.999V range. For maximum accuracy, there should be provision for adjustment to either of these values.
7	V_{DD}	Positive supply voltage. +5.0V is recommended; +6.5V is maximum.
8	CL1	External clock input. To use internal clock, see Freq. Setting.
9	CL2	If external clock is connected to pin 8, leave open. To use internal clock see Freq. Setting.
10	CL3	If external clock is connected to pin 8, leave open. To use internal clock see Freq. Setting.
11	A.	The multiplexed BCD outputs are on pins 11 (least significant bit) through 14 (most significant bit). Drive capability is one TTL load. These logic levels change state simultaneously and without a blanking period. to the BCD code corresponding to the next digit. This change of state is synchronized with digit select signals on pins 15 through 18.
12	B.	See pin 11.
13	C.	See pin 11.
14	D.	See pin 11.
15	10^0(LSD)	Digit select signal. A logic "1", 8 clock cycles in duration, selects the rightmost or least significant digit. Similar pulses on each of pins 15 through 18 are separated in time by blanking periods of 2 clock cycles. These pulses select each digit in sequence, LSD through MSD. See Multiplex Timing.
16	10^1	See pin 15.
17	10^2	See pin 15.
18	10^3(MSD)	See pin 15.
19	GND	Digital ground. Connect to analog ground, pin 2.
20	+POL	Polarity output, with logic "1" for negative V_{IN}.
21	HOLD	Display hold input. Logic "1" allows update of the display; logic "0" freezes the display. This has no effect on the conversion cycle. An internal pull-up resistor assures an update for each cycle when no connection is made to this pin.
22	C.	Capacitor for auto-zero and noise-supression, connected between pin 22 and pin 2. A 0.1μF low leakage type is recommended.
23	EOC	Positive transition indicates conversion is complete and new cycle is beginning. The pulse stays high while V_{IN} is being integrated.
24	V_{SS}	Negative supply voltage, -5.0V is recommended; -9.0V is maximum.
25	I_O	Integrator output. Connect a mylar capacitor from pin 25 to pin 26. Recommended value is 0.1μF ±10%.
26	SUM	Integrator summing junction.
27	BO	Buffer output. A resistor from this pin to pin 26 provides input to the integrator. Resistor value depends on the input range: 100K ±10% 199.9mV range 1M ±10% 1.999V range
28	C_{AZ}	Auto-zero capacitor. See pin 1.

3-1/2 Digit DPM (Single Power Supply)



NOTES:
*METAL FILM RESISTOR
**MYLAR FILM CAPACITOR

THESE COMPONENTS ARE NOT REQUIRED IF A NEGATIVE SUPPLY VOLTAGE IS PROVIDED.

Figure 1.

Design Information

DPM, Minimum Connections

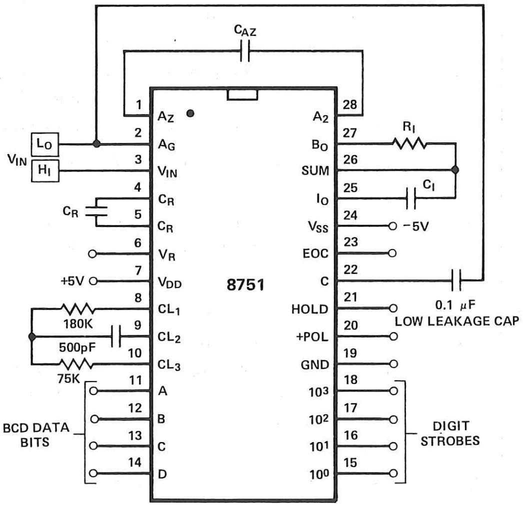
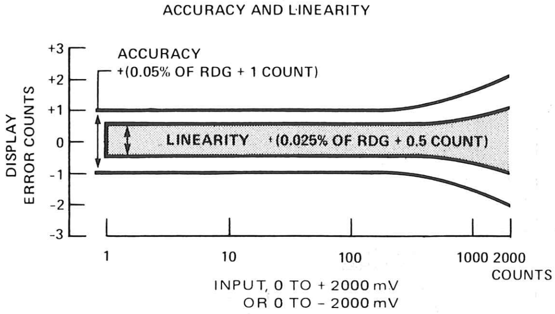


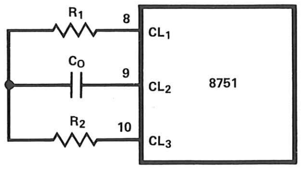
Figure 2.

FULL SCALE			
	2V	200mV	
†C_{AZ}	0.1μF	0.47μF	MYLAR CAPACITOR OR POLYPROPYLENE CAPACITOR
†C_R	0.22μF	0.47μF	
C_I	0.1μF	0.1μF	
R_I	IMΩ	100KΩ	±10%
V_R	I_V	100mV	

† Higher value gives better performance.



Frequency Setting



Frequency of the internal clock oscillator is set by R_2 and C_0, according to the approximate formula shown below. The primary purpose of R_1 is to limit the signal current into pin 8. Its value is not critical and it has little effect on clock frequency.

EXAMPLE:

$$f_{CLK} = \frac{1}{2.2\ R_2\ C_0} = \frac{1}{2.2 \times 86K \times 500pF} = 10\ KHz$$

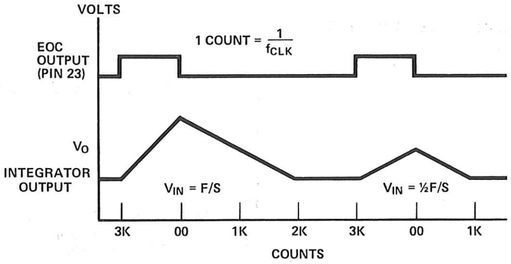
$R_1 = 180K$
$R_2 = 86K$
$C_0 = 500pF$

One TTL equivalent load or less may be connected to pin 10, to provide drive for a negative voltage supply or other external circuit. See Figure 1. If an external clock signal is connected to pin 8, then pins 9 and 10 should be left open.

Determination of R_1 and C_1

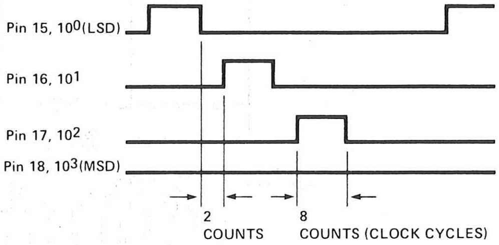
The input voltage, clock frequency, and integrator components R_1 and C_1 are related as shown below. C_1 should be a low leakage mylar type, but component values are not critical. For best performance use values as shown in Figure 2. Also, with ±5V supplies, the internal integrator output voltage V_0 should not exceed 2.4 volts.

$$V_0 = \frac{10^3\ V_{IN}}{R_1\ C_1\ f_{CLK}} \leqslant 2.4V$$

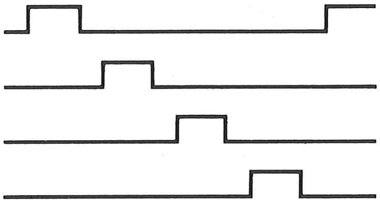


Multiplex Timing

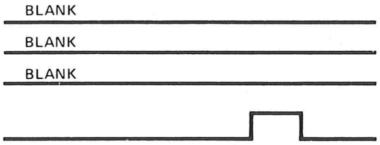
The digit select signals on pins 15 through 18 assume three different patterns, depending on magnitude of the voltage being displayed. On the 2V range for example, only the three rightmost digits are displayed for inputs less than one volt:



For an input between 1 and 2 volts (more precisely, an input producing between 1000 and 1999 counts at the integrator), the leftmost digit also is displayed:

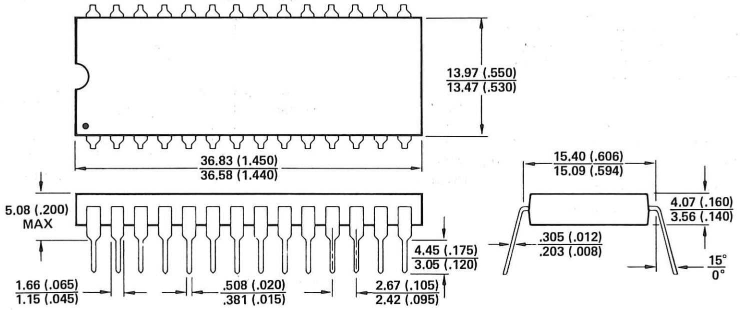


If the input is 2.0 volts or greater (⩾ 2000 counts) the three rightmost digits are blanked to indicate an overrange condition: (Pins 15, 16 and 17 stay low)

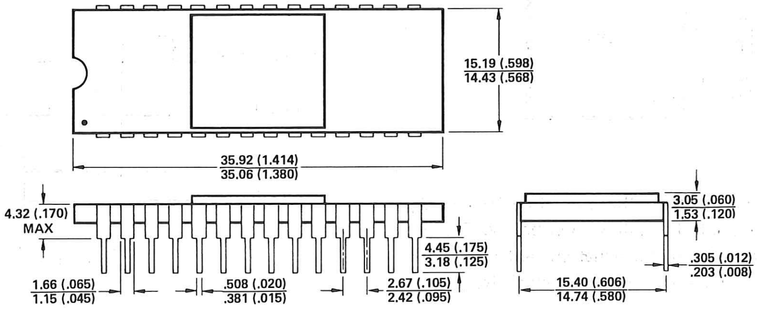


Physical Dimensions

J Package 28–Pin Plastic



N Package 28–Pin Ceramic



Note: 1. Pin 1 identified by adjacent dot, indent or end notch.
2. Dimensions in millimeters (inches).

II

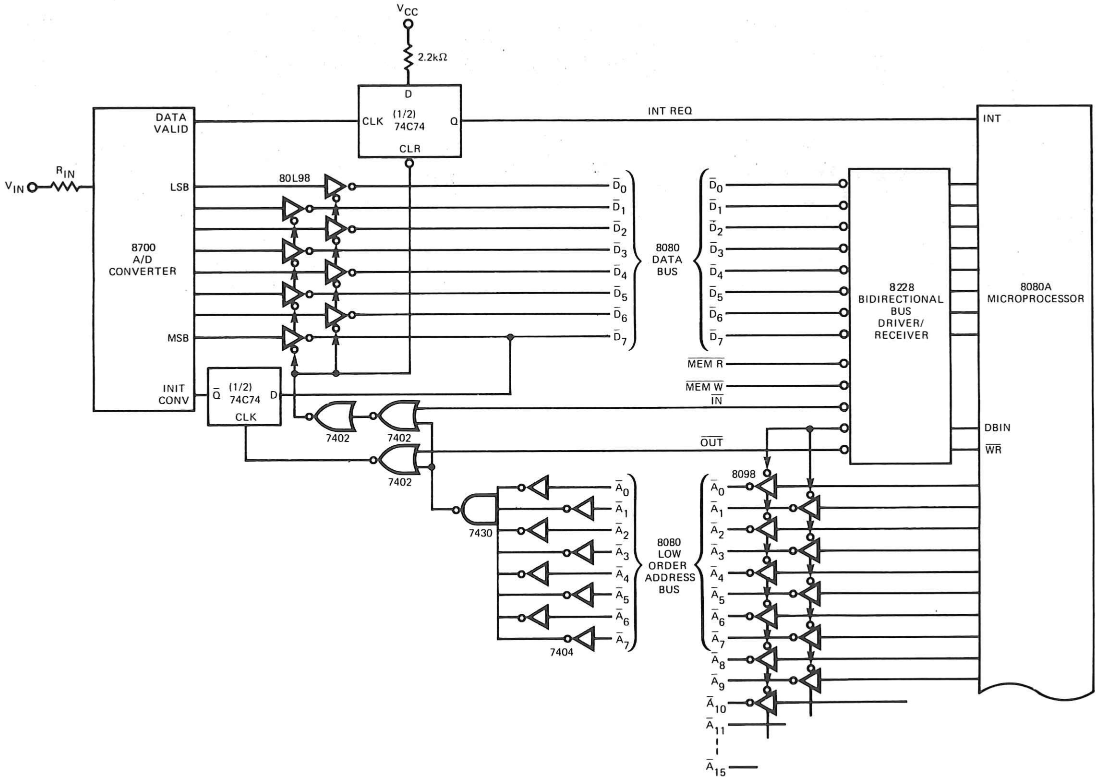
Monolithic CMOS A/D Converters

Application Notes

Interfacing the 8700 A/D Converter with the 8080 μP System

AN-8

Dave Guzeman
August 1976



INTERFACING THE 8700 A/D CONVERTER WITH THE 8080 μP SYSTEM

The growth of microcomputers has included an expansion into process monitoring and control systems, as well as other applications requiring interaction with "real world" physical variables. At the same time, advances in semiconductor technology have allowed complex data conversion functions (A/D, D/A, V/F, etc.) to be performed by small and inexpensive IC's. By integrating these monolithic converter circuits into his microcomputer system, the designer thus can retain the same low cost and small size advantages which make the microprocessor so attractive.

In particular, the popular Intel 8080A microprocessor and Teledyne Semiconductor's 8700 series analog-to-digital converters are well suited to such a combination. This paper describes the basic techniques for interfacing the two, as well as ways to handle some more sophisticated situations.

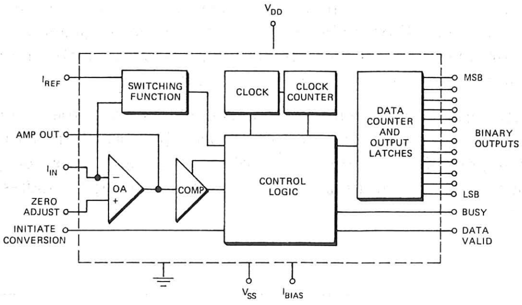


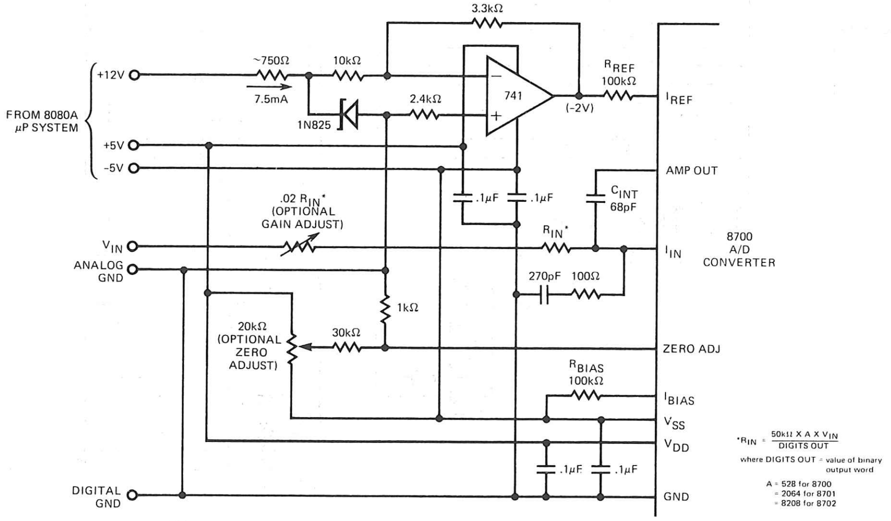
Figure 1. 8700 Series Internal Elements

THE 8700 A/D CONVERTER

Teledyne Semiconductor's 8700 series is a family of monolithic CMOS analog-to-digital converter IC's. All versions – the 8700 8-bit, 8701 10-bit and 8702 12-bit – are integrating converters which can accept an unlimited input voltage range (changed to a current input by external scaling resistor) and provide a latched parallel binary digital output. All are available in 24-pin ceramic DIP, and the 8-bit version is also offered in a low-cost 24-pin plastic package. As may be seen from the block diagram (Fig. 1), each device contains all of the essential elements for a complete A/D converter; only minimal support components are needed.

In addition to the 8, 10 or 12 buffered data output lines, three handshaking signals are provided to ease the interface to the host system. All outputs are CMOS and LPTTL compatible. The DATA VALID output signal is normally high, indicating that the data in the output latches is valid, for the entire cycle except for approximately 5μs before the end of the conversion, when the data is being updated. Notice that the latches maintain the data from the previous conversion even while the next conversion is being performed. A second output, BUSY, is high whenever a conversion is being performed. Finally, an input to the device, INITIATE CONVERSION, allows the function to be operated under system control. A positive-going pulse of at least 500ns duration causes the conversion to begin. If this input is tied high, the conversion will occur in a free-running mode at approximately 800 conversions per second for the 8700 (200 conv/sec for the 8701 and 50 conv/sec for the 8702).

Since the 8700 series devices operate from +5V and -5V supplies, they are particularly easy to interface with the 8080A microprocessor system. Fig. 2 shows a possible hook-up for the 8700's analog inputs and power supply; also



$$^{*}R_{IN} = \frac{50k\Omega \times A \times V_{IN}}{\text{DIGITS OUT}}$$

where DIGITS OUT = value of binary output word

A = 528 for 8700
= 2064 for 8701
= 8208 for 8702

Figure 2. 8700 Analog Input and Power Supply Hook-up Circuits, Including V_{REF} Derived from 8080A System

incorporated is a circuit to supply the necessary negative reference, using a temperature-compensated zener diode and an inverting op amp. Note that the ±5V supplies needed for the 8700, as well as the additional +12V used in the reference circuit, are all available from the 8080A system.

In order to simplify the hardware and software for illustrative purposes, this paper concentrates on interfacing the 8-bit 8700 converter and the 8-bit 8080A microprocessor system. The same principles apply to inter-connecting the 8080A with the higher-resolution 8701 and 8702 A/D converters.

THE 8080A MICROPROCESSOR

The 8080A, an 8-bit microprocessor, communicates within the microcomputer system over two buses, a 16-bit address bus and an 8-bit data bus. During each machine cycle the current contents of the program counter are sent out over the address bus; the memory receives the address and returns the contents of the selected memory location to the 8080A via the data bus. During an instruction fetch cycle, the returning data is interpreted as an instruction.

Communications between the microcomputer and the outside world are via Input/Output (I/O) ports addressed by the address bus. I/O instructions utilize 8-bit addresses; the port address is duplicated on both the low order address lines and the high order address lines of the address bus.

In addition to the address and data buses, the 8080A communicates with the memory and I/O ports via a set of control signals. In particular two control lines, $\overline{\text{IN}}$ and $\overline{\text{OUT}}$, are used to enable the I/O ports. A logic 0 on the $\overline{\text{IN}}$ line will enable the Input port that corresponds to the address on the address bus at that time. The $\overline{\text{OUT}}$ line functions in a similar fashion.

THE BASIC 8700 I/O PORT

A basic approach to interfacing the 8080A and the 8700 8-bit A/D converter is shown in Fig. 3. The conversion is started on command of the 8080A, using the INITIATE CONVERSION input of the 8700. When the conversion is complete, the DATA VALID output of the A/D requests an interrupt; the interrupt service routine transfers the current data from the working registers to the stack memory, and the A/D input port is read. A control signal then is sent to the INITIATE CONVERSION input to restart the conversion, and the main program activity is resumed.

It is assumed that the data bus will be shared by many devices, both in the ports and in memory, and that inverting drivers/receivers (such as 8228) will be included in the 8080A system to service this bus. Therefore, 80L98 buffers have been provided at the 8700 to drive an inverted input over the data bus, as well as to provide a three-state function, electrically removing the A/D from the bus when its input port has not been selected. (For applications where inverted signal and high bus-driving capability are not needed, Teledyne is offering a version of the 8700 with three-state outputs.)

Each port of the system is assigned an address by virtue of the way the address bus is decoded to select the port. In the basic input port of Fig. 3, the output of the 7430 gate is low only when all of its inputs are high. This corresponds to address FF$_H$.

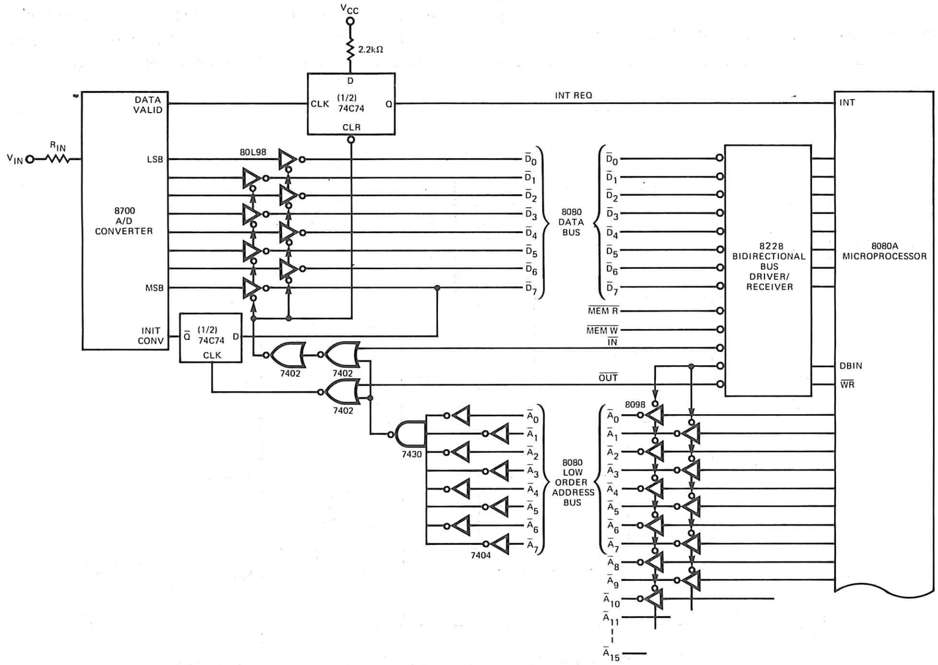


Figure 3. Basic 8700/8080A Interface

```
;INITIATION
        MVI     A,80H   ;THE CONVERSION
        OUT     0FFH    ;IS INITIATED
        MVI     A,0     ;BY SENDING A
        OUT     0FFH    ;BRIEF PULSE
                        ;TO PORT FF
;INTERRUPT
        PUSH    B       ;THE PROCESSOR
        PUSH    D       ;REGISTERS AND
        PUSH    H       ;STATUS ARE SAVED
        PUSH    PSW     ;IN THE STACK, AND THE
        IN      0FFH    ;DATA IS READ AND
        MOV     B,A     ;STORED IN REG B.
        MVI     A,80H   ;THE CONVERSION IS
        OUT     0FFH    ;INITIATED AND
        MVI     A,0     ;THE DATA IS
        OUT     0FFH    ;PROCESSED.
        •
        •
        •
        •
        POP     PSW     ;WHEN COMPLETE,
        POP     H       ;THE REGISTERS
        POP     D       ;ARE RESTORED, THE
        POP     B       ;INTERRUPTS ENABLED
        RET             ;AND PROGRAM
                        ;CONTROL RETURNED
                        ;TO THE MAIN PROGRAM.
```

Figure 3A

To initiate a conversion in the A/D, an output port, also address FF_H, is used. By defining both the input and output ports as address FF_H, the same address decoder, the 7430, may be used for both functions. In this case the output of the 7430 and the $\overline{OUT}$ signal are gated by 7402 to clock half of a 74C74 flip-flop. The D input of the flip-flop is tied to the D_7 line of the data bus. The flip-flop is, in effect, a one-bit output port. Sending the data word 80_H to port FF_H with an output (OUT) instruction will cause the flip-flop to be set, thus supplying an INITIATE CONVERSION signal to the 8700. A second output instruction, sending 00_H to the same port, will reset the flip-flop and remove the INITIATE CONVERSION signal. Since an output instruction requires ten 0.5μsec clock cycles to execute, the INITIATE conversion pulse will be approximately 5μsec long. After beginning the conversion process by the double output instructions, the 8080A is free to perform other processing operations.

When the 8700 completes its conversion cycle and latches the result onto its internal output latches. the DATA VALID output goes high. This triggers the other half of the 74C74 flip-flop, clocking a logic one from the D input (tied high) onto the INTERRUPT REQUEST line. The result is that the microprocessor is interrupted when the conversion is complete. The interrupt service routine (See Fig. 3A) saves the CPU's working register contents by pushing them onto the stack and then reads the output of the 8700.

To read the 8700 input port, it is necessary to supply the address of port FF_H on the address bus while simultaneously sending out a logic zero on the $\overline{IN}$ control line. The combination of the 7430 and 7402 gates supplies a logic zero to the enabling input of the 80L98 three-state buffers on the outputs of the 8700 and to the clear input of the 74C74 flip-flop on the INTERRUPT line; this puts the 8700 data on the data bus and removes the interrupt request.

After reading the converter data and saving it in one of the registers, the system again pulses the INITIATE CONVERSION input to start the next conversion, restores the stack with a series of POP instructions, and resets the internal interrupt-enable flip-flop. Thus the 8080A only reads the 8700 when the new information becomes available; the rest of the time is spent in processing activities.

HANDLING MULTIPLE A/D CONVERTERS

When multiple analog inputs are involved, conventional system designs have tended to use an analog multiplexer feeding a single high-speed A/D converter. With the increasing availability of low-cost converter IC's, the approach of using a separate A/D for each analog line becomes more attractive. Fig. 4 illustrates a system of eight 8700 converters all supplying data in parallel to an 8080A system.

The system illustrated in Fig. 4 contains many of the same elements as the basic input port of Fig. 3. As before, the data outputs of the 8700s are buffered with 80L98 three-state buffers to drive the bus and to allow them to be disconnected. The decoding circuitry is slightly more complex. The five high-order address lines form the inputs to a 7430 gate which is used to enable a 7442 BCD to decimal decoder. The 7442 performs the final decoding by selecting the appropriate 8700 whenever an INPUT instruction is executed to one of the output ports $F8_H$ to FF_H. Also, the 8700s have their INITIATE CONVERSION inputs tied high so the devices operate in the free-running mode.

The interrupt scheme in this system is far more versatile than that previously illustrated. The user may assign priorities to each of the input ports, so that if one port has already interrupted the system and is being serviced, only a higher priority port can interrupt it. Lower priority interrupts will be delayed until the first port has been serviced.

Each of the eight interrupt input ports is constructed of a 74L74 flip-flop with its D inputs wired high. Each flip-flop is clocked independently by lines from the appropriate 8700 DATA VALID output, transferring the logic one on the D input to the Q output. The $\overline{Q}$ output of each flip-flop is gated onto the $\overline{INT\ REQ}$ line producing an interrupt whenever one of the 8700's completes its cycle. The Q outputs of the flip-flops are buffered by the 8098 and tied to the data bus; this buffer is enabled by a 7430 and 7400 gates to respond to the INPUT instruction at address $7F_H$. The 8080A thus can determine which flip-flop has caused the interrupt and which of the 8700s has completed its conversion cycle.

The interrupt service routine (See Fig. 4A) saves the contents of the working registers with a series of PUSH instructions, and then proceeds to determine which port caused the interrupt. This is done with an input ($\overline{IN}$) instruction to address $7F_H$, which loads the status of the DATA VALID outputs from the 8098 into the accumulator. Here the word can be tested, bit by bit, until a logic one is found. This is then converted to the address of the correct 8700 input port and that port read with an input instruction. At the conclusion of the service routine, the flip-flop is reset by sending a zero to the appropriate bit position of the output port $7F_H$ which shares the same decoding circuitry as the input status port. Finally the stack is restored, and the internal interrupt enable flip-flop is reset.

There is nothing to prevent one of the 8700s from completing its conversion cycle and sending out a DATA VALID signal at the very time that another 8700 port has caused an interrupt and is in the process of being read. If this occurs, the flip-flop tied to the second port will be set and an additional interrupt signal generated. This will have no effect, however, since the

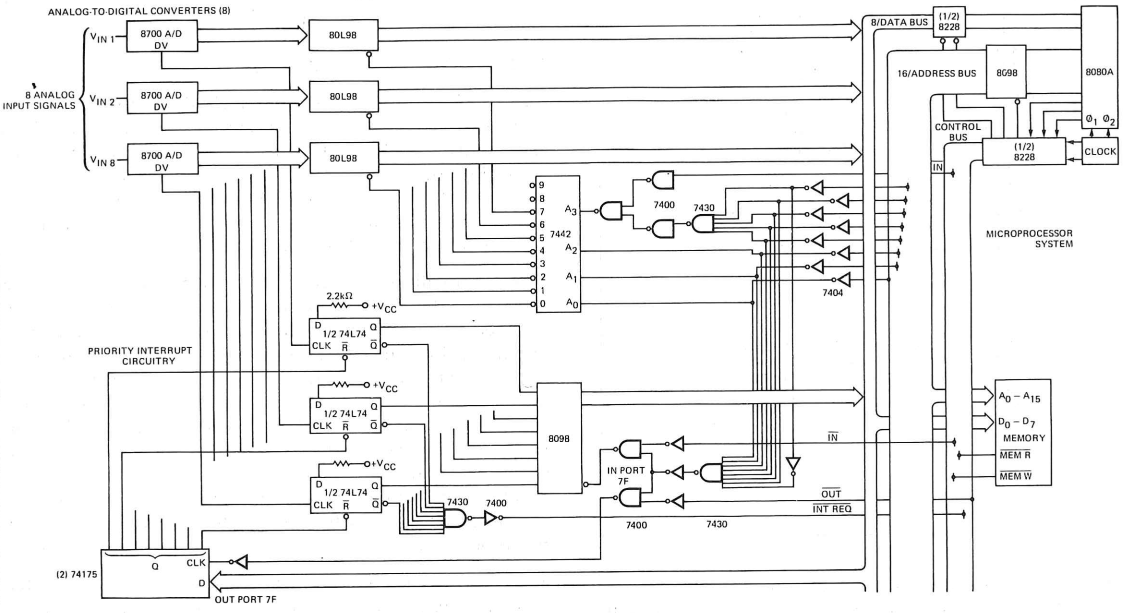


Figure 4. Eight Port A/D Converter System with Maskable Priority Interrupt

```
;THIS IS A PROGRAM FOR RESPONDING
;TO AND SERVICING EIGHT INTERRUPTING
;INPUT PORTS ON A PRIORITY BASIS.
POLLED: PUSH    B       ;SAVE PROCESSOR
        PUSH    D       ;REGISTERS AND
        PUSH    H       ;STATUS.
        PUSH    PSW
        IN      7FH     ;READ INPUT PORT
        MVI     D,0     ;TO FIND WHICH
        STC             ;CAUSED INTERRUPT.
        CMC             ;SET D TO ZERO
                        ;AND CARRY TO ZERO.

LOOP1:  RAL             ;DETERMINE WHICH
        INR     D       ;PORT CAUSED INTERRUPT
        JNC     LOOP1   ;BY ROTATING ACCUMULATOR
                        ;LEFT AND TESTING
                        ;FOR PRESENCE OF
                        ;CARRY.  INCREMENT
                        ;D EACH TIME.
        LXI     H,STABL ;LOAD H AND L WITH
        LXI     B,3     ;STARTING ADDRESS
                        ;OF JUMP TABLE AND
                        ;B AND C WITH 3.

LOOP2:  DAD     B       ;ADD B AND C TO
        DCR     D       ;H AND L, DECREMENT D
        JNZ     LOOP2   ;AND TEST FOR
        PCHL            ;ZERO.  EXIT LOOP
                        ;BY TRANSFERRING
                        ;TO APPROPRIATE
                        ;JUMP COMMAND
                        ;IN JUMP TABLE.

STABL:  JMP     ONE     ;JUMP TABLE
        JMP     TWO     ;CONSISTING OF
        JMP     THREE   ;3-BYTE JUMP
        JMP     FOUR    ;INSTRUCTIONS.
        JMP     FIVE
        JMP     SIX
        JMP     SEVEN
        JMP     EIGHT
```

```
RSTR:   POP     PSW     ;RESTORE REGISTERS
        POP     H       ;AND EXIT.
        POP     D
        POP     B
        RET
ONE:    IN      0F8H    ;THIS IS THE
        MOV     B,A     ;SERVICE ROUTINE
        MVI     0FEH    ;FOR PORT #1.
        OUT     7FH     ;IT LOADS THE
        EI              ;PRIORITY MASK.
        .               ;WITH 1111 1110,
        .               ;ENABLES INTERRUPTS
        .               ;AND PROCESSES
        .               ;DATA.  AT CONCLUSION,
        .               ;THE PROGRAM JUMPS
        JMP     RSTR    ;TO RSTR.

TWO:    IN      0F9H    ;THIS IS THE
        MOV     B,A     ;ROUTINE FOR
        MVI     0FCH    ;PORT #2.  THE
        OUT     7FH     ;PRIORITY MASK
        EI              ;IS 1111 1100 WHICH
        .               ;KEEPS PORT #1
        .               ;FROM INTERRUPTING.
        .
        .
        .
        JMP     RSTR
;THE BALANCE OF THE SERVICE ROUTINES
;ARE OMITTED FOR BREVITY.
```

Figure 4A

8080A's internal-interrupt enable flip-flop is automatically disabled when the first interrupt is received, locking out any further interrupts. (This flip-flop must be reset with an EI instruction, Enable Interrupts.) The first interrupt service routine ends with the resetting of the status flip-flop and the enabling of the internal interrupt enable flip-flop. This removes the source of the first interrupt, but the second status flip-flop now causes a new interrupt which must be serviced in turn. The 8080A will respond to each of the input ports as they complete their cycles, even if several occur in a short period.

So far we have assumed that each of the 8700 ports is of equal importance. When we wish to assign priorities to the ports, it is only necessary to make a slight change in the program — no hardware changes are needed. This is done by holding the reset inputs of selected data valid flip-flops low, which effectively serves to inhibit those ports from causing interrupts. The output port 7F accomplishes this by having its latches loaded with a binary word called a priority mask. Each interrupt service routine begins by loading a different priority mask into the output port and resetting the internal enable interrupt flip-flop. For example, if the priority mask for port number 3 is 11111100, port number 1 and 2 cannot interrupt the processing of port number 3 data; ports number 4 through number 8, however, can cause further interrupts.

If it is necessary to guarantee that no data is ever lost, a slight modification places the conversion cycle under the control of the CPU. This is done by tying the reset inputs of the status flip-flops to the INITIATE CONVERSION inputs of the corresponding 8700's. The process of resetting the status flip-flop after the port has been read will cause the cycle to restart. This has the effect of holding the data on the output latches of the 8700's until it has been read.

INCREASING THE THROUGHPUT

If a great deal of data manipulation is to be done by the 8080A or a large number of 8700 input ports are to be connected to the bus, it is possible to feed data to the system faster than it can be processed. If the analog inputs on some of the ports are changing slowly, additional logic can be added to increase the effective capacity of the system. This involves adding a latching output port with the same address as the 8700 input port corresponding to it. (See Fig. 5) After the input port is read initially, an output instruction to the same address causes the data to be duplicated in the 74175 latches. The open collector feature of the 9386 allows them to be collector-ORed; logic ones at all of their outputs signify that the data in the 8700 latches matches that in the output port. This condition means there has been no change in the analog input voltage and there is no need to reprocess the data. If one of the bits of the 8700 does not match the corresponding bit in the 74175, a zero will be produced on the outputs of the 9386. This will deliver a clock pulse to the 7474 status flip-flop which will in turn interrupt the 8080A. From this point the operation is similar to the system already discussed.

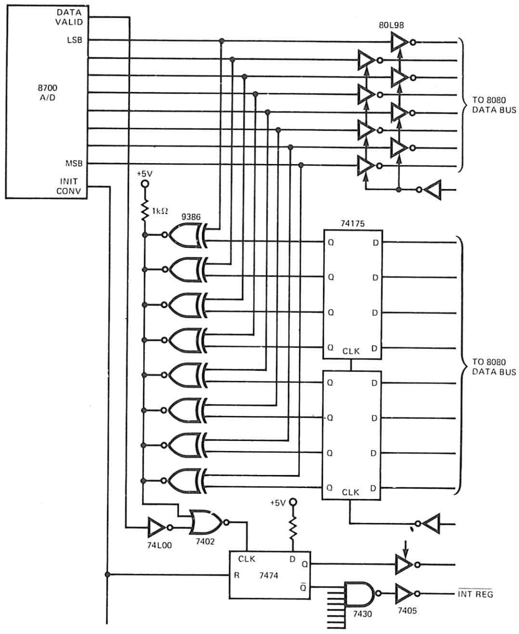


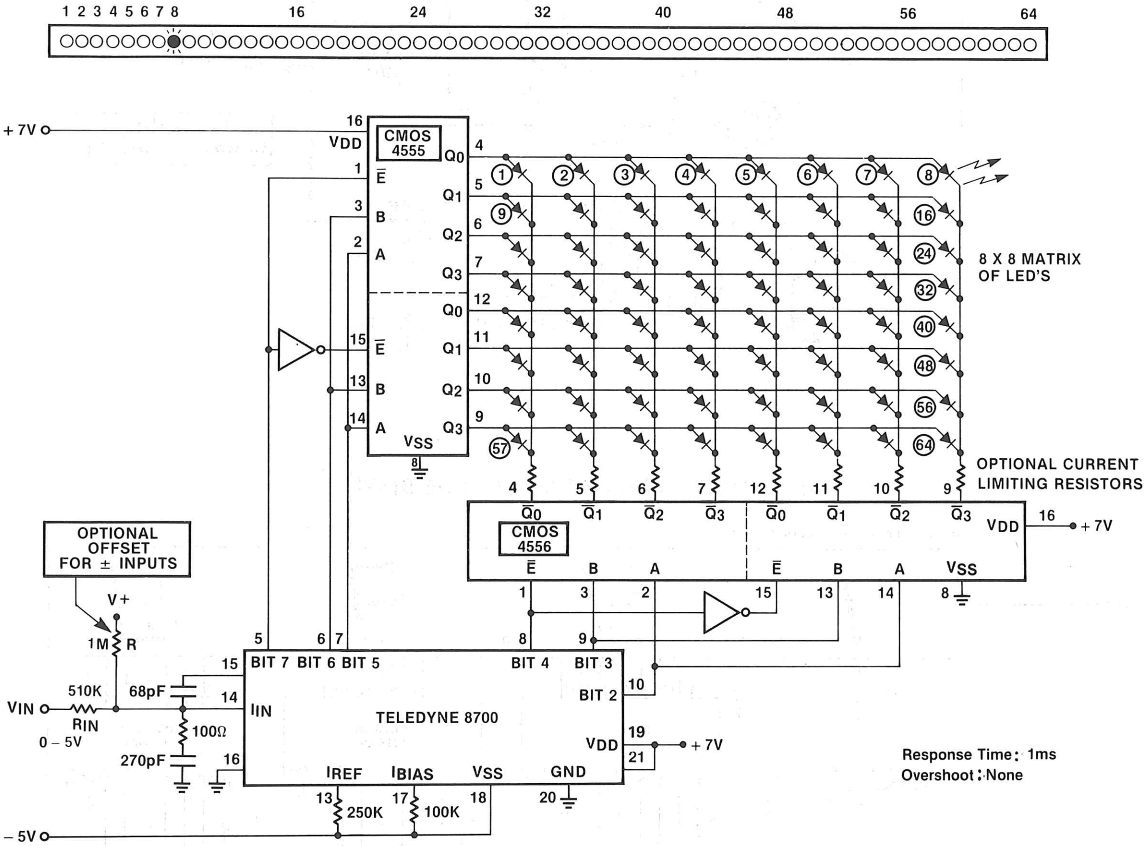
Figure 5. Significant Change Interrupt for 8700 Input Port

Applications of the 8700 Series CMOS A/D Converters

AN-9

Michael O. Paiva
John Blake
September 1978

LED PANEL METER



Response Time: 1ms
Overshoot: None

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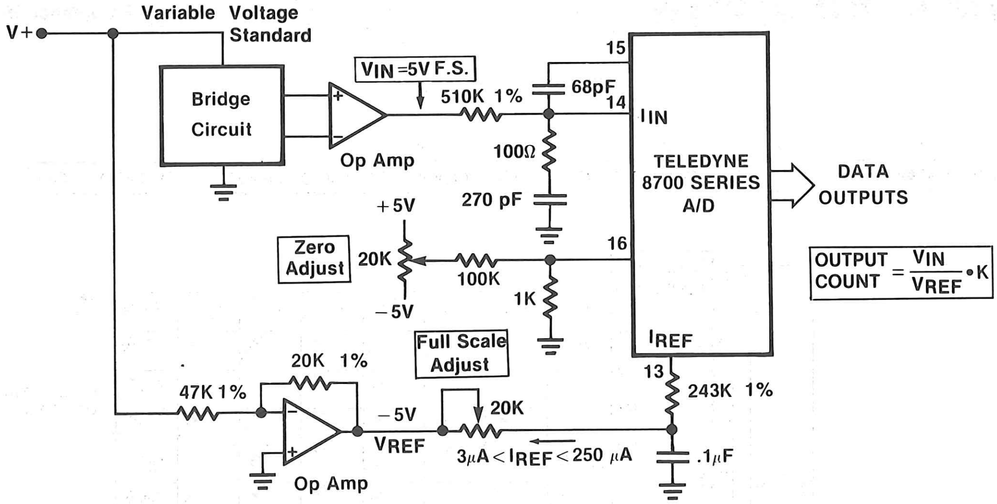
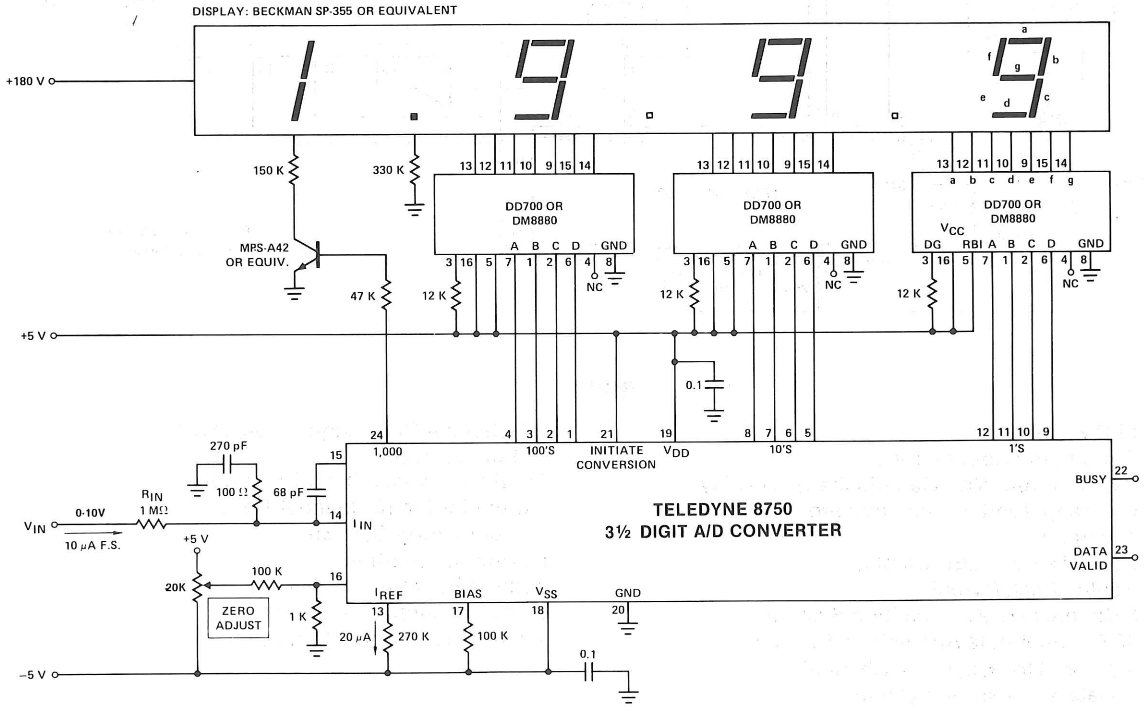
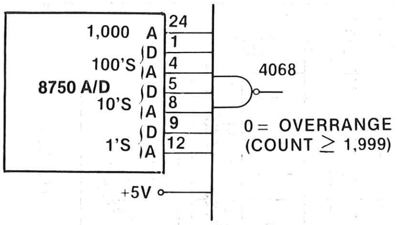
RATIOMETRIC APPLICATIONS



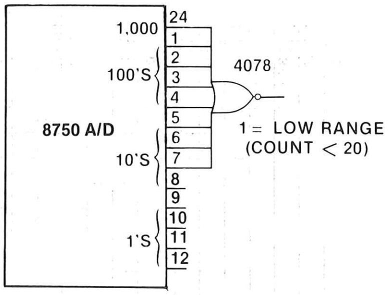
3½ DIGIT A/D WITH GAS DISCHARGE DISPLAY



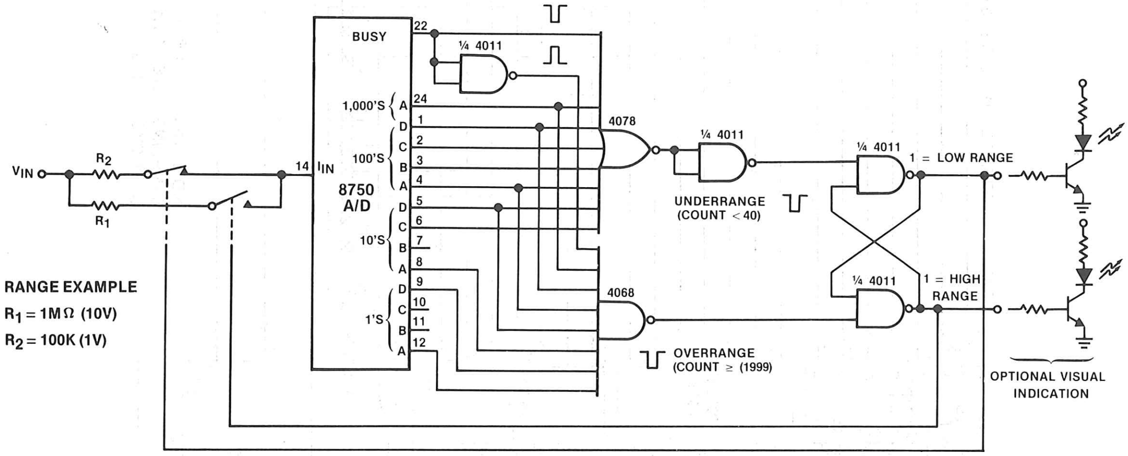
OVERRANGE INDICATOR



UNDERRANGE INDICATOR

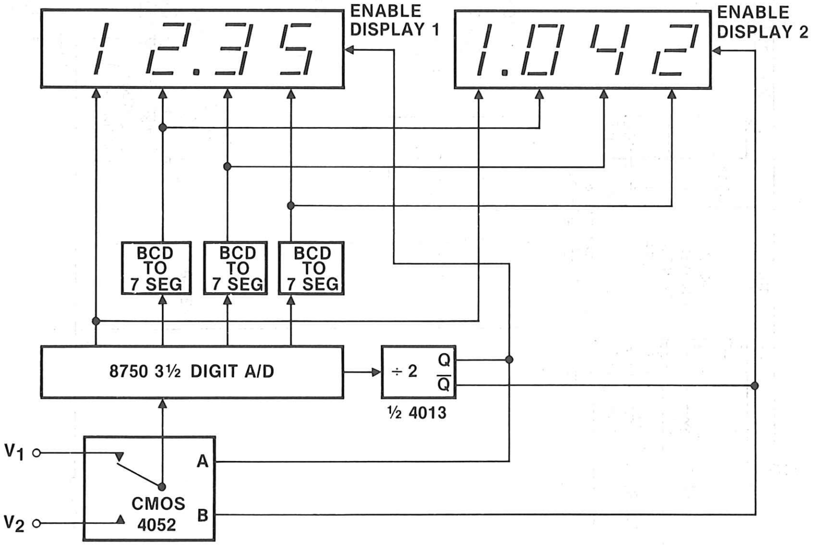


A/D WITH TWO STEP AUTORANGE

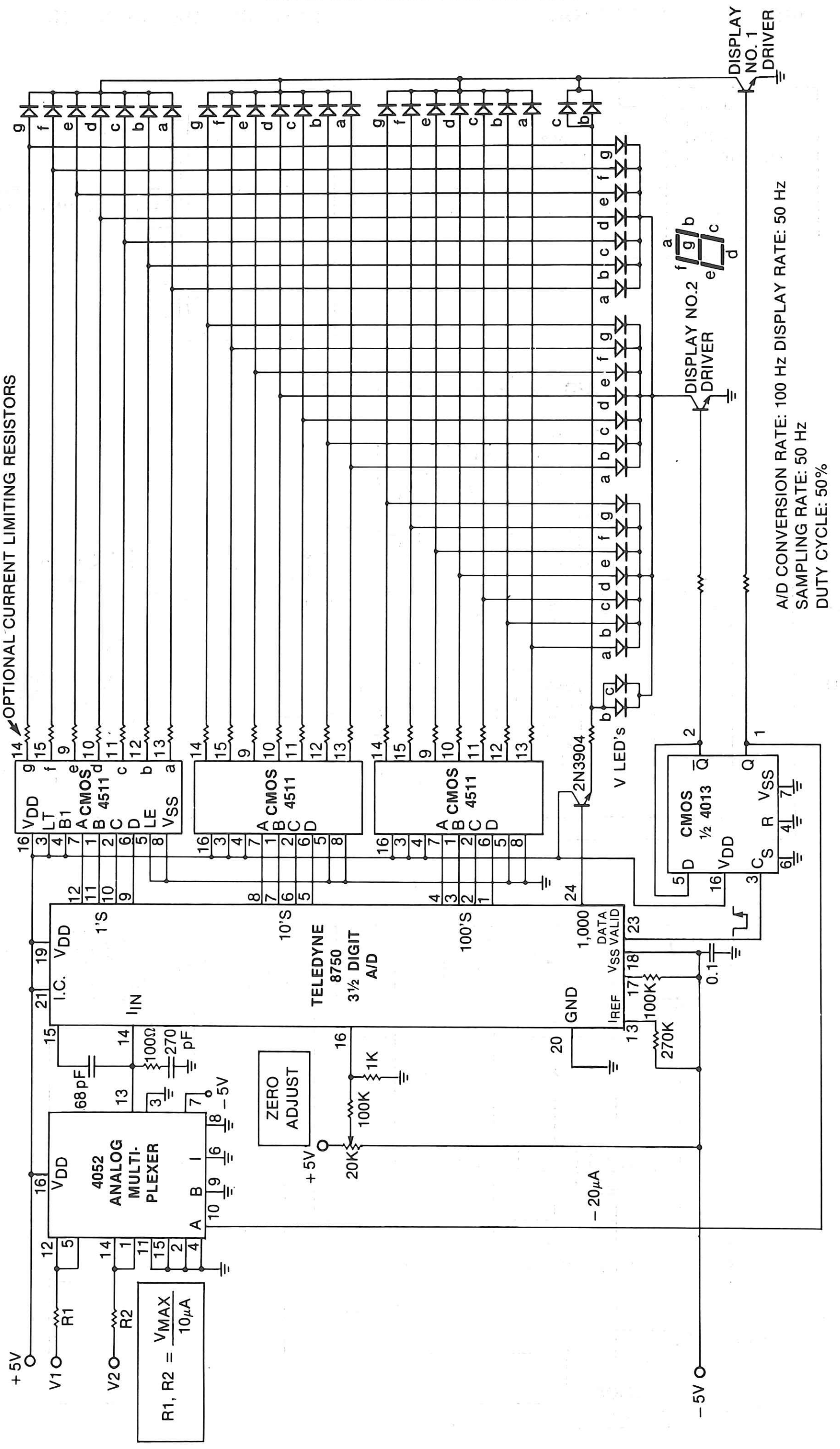


RANGE EXAMPLE
R$_1$ = 1MΩ (10V)
R$_2$ = 100K (1V)

DUAL 3½ DIGIT LED DISPLAY

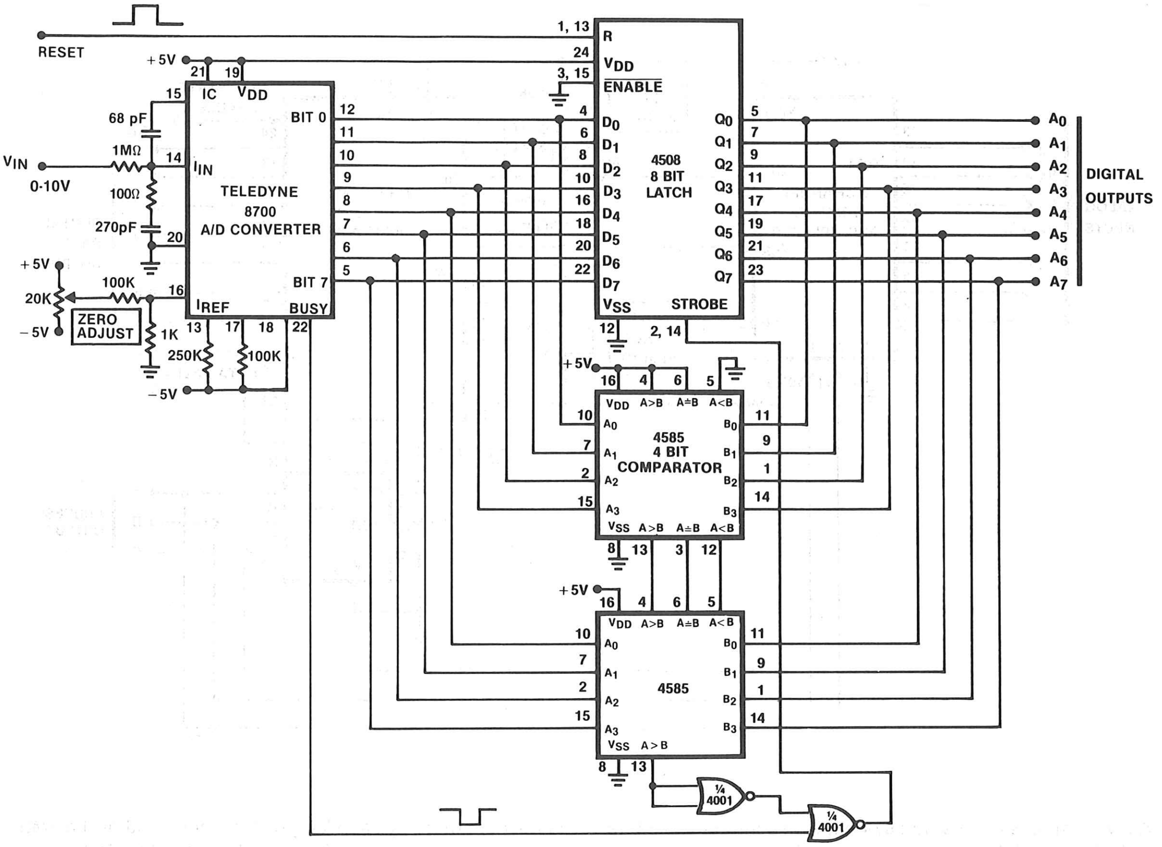


DUAL 3½ DIGIT LED DISPLAY



A/D CONVERSION RATE: 100 Hz DISPLAY RATE: 50 Hz
SAMPLING RATE: 50 Hz
DUTY CYCLE: 50%

ANALOG PEAK DETECTOR WITH DIGITAL HOLD

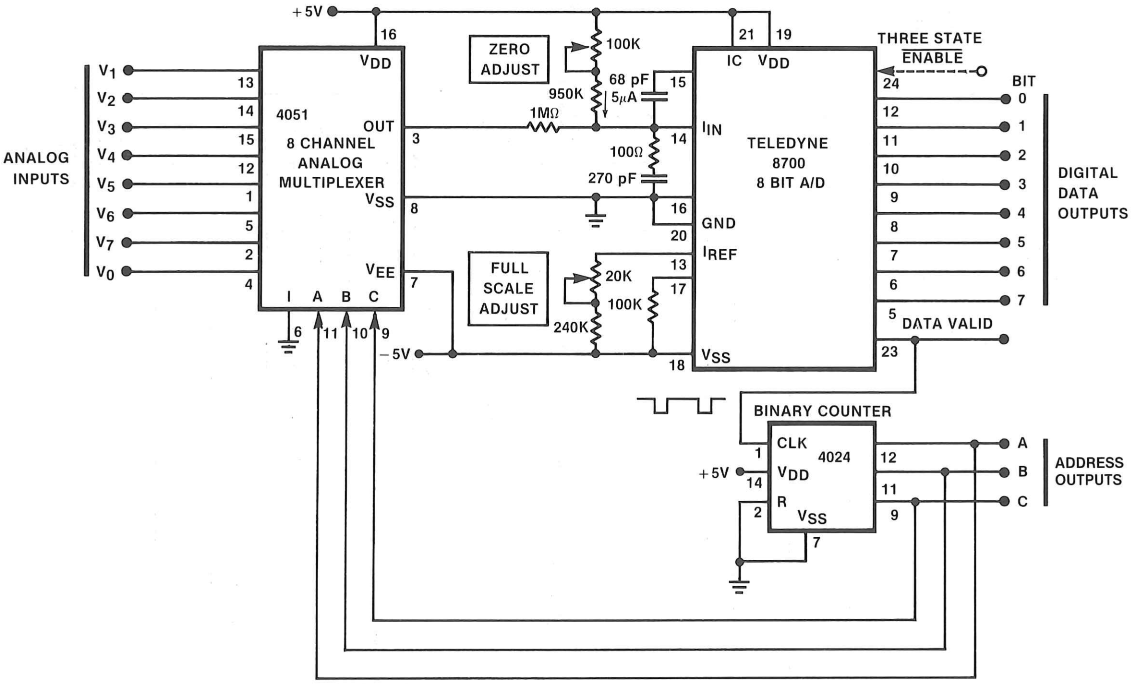


Analog peak detection is accomplished by repeatedly measuring the input signal with an A/D converter and comparing the current reading with the previous reading. If the current reading is larger than the previous, the current reading is stored in the latch and becomes the new peak value. Since the peak is stored in a CMOS latch, the peak can be stored indefinitely.

The TELEDYNE 8700 A/D converter measures the analog input at a 1 KHz rate and computes the binary value of the input. After each 1ms measurement, the binary value is latched in the output of the A/D. This value is then presented to both the 4585 comparators and the 4508 8-bit latch. If the A/D's value is greater than that of the 4508 memory, pin 13 (A>B) of the 4585 goes high. This allows the strobe pulse to go through the 4001 NOR gate to the 4508 memory. The new value is then stored and becomes the reference for subsequent readings. Each time the A/D has a value greater than that stored in the latch, the latch is updated with the larger peak. The system is reset by pulsing the 4508 reset pin high, causing the output to go to 0000 0000.

This system uses an 8-bit A/D to give 0.4% resolution. If greater resolution is required, the 8700 can be replaced by the 8701 (10-bit) for 0.1% resolution or the 8702 (12-bit) for 0.025% resolution. Since this will require 10 or 12 bits to be compared instead of 8, the memory and comparator need to be expanded by adding one additional 4508 and one 4585.

8—CHANNEL DATA ACQUISITION SYSTEM



A low-cost data acquisition system with 8 inputs and 8 bits (0.4%) of resolution at the ouput can be built by using the TELEDYNE 8700 CMOS A/D converter and adding the 4051 8 channel CMOS multiplexer and the 4024 binary counter.

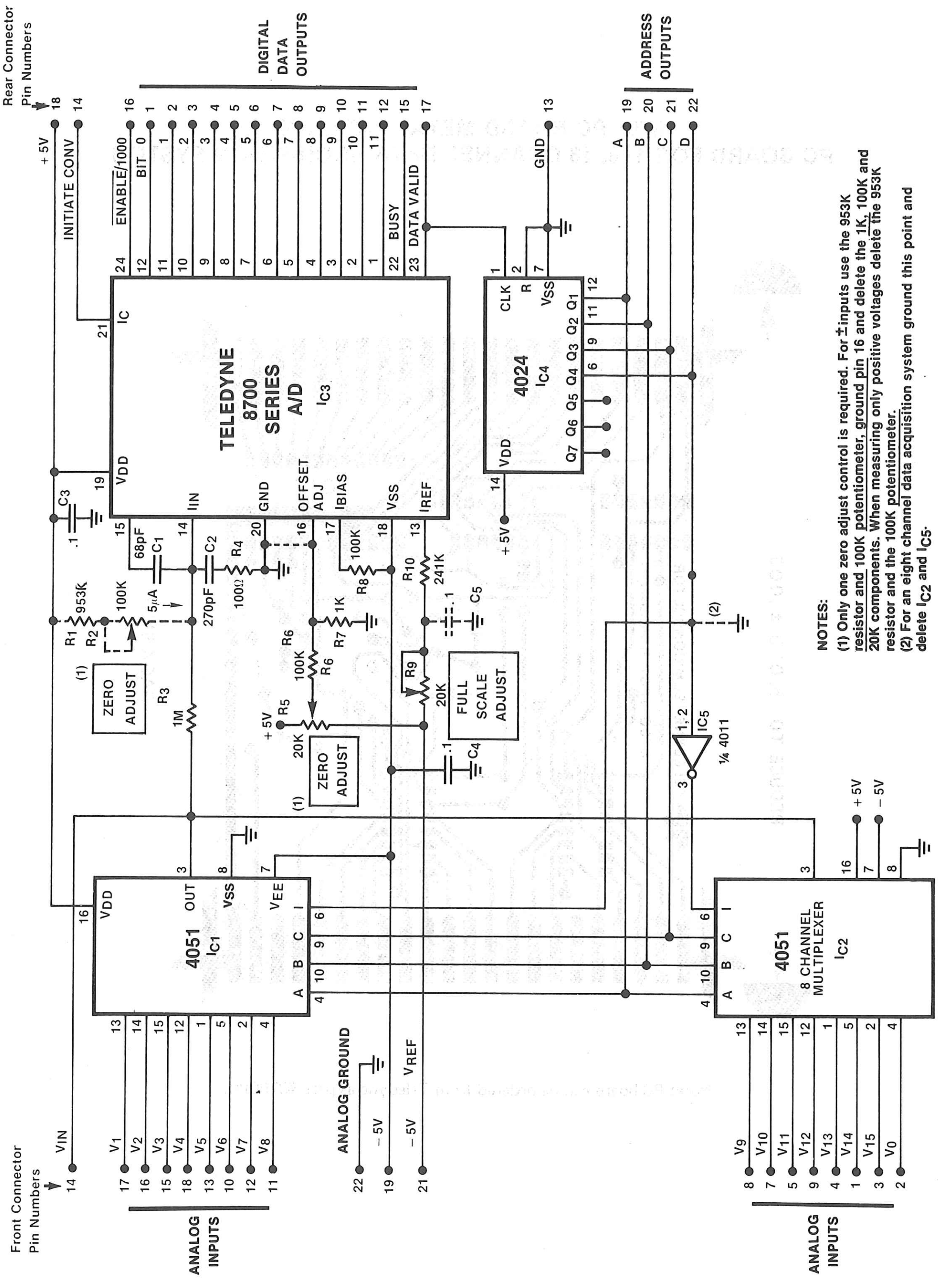
Each input is measured for 1ms, then the digital value is placed in the output latch and remains for 1ms while the next input is being measured. After each 1ms measurement (conversion), the data valid line goes low for 5μs to indicate that the output latch is being updated. (The data must not be read during this period.) The negative edge of the data valid pulse is used to advance the binary counter by one. So after each conversion the 4051, via the 4024, automatically advances to the next input. The sampling sequence is therefore V_1, V_2,...V_7, V_0 and then back to V_1. The 8700 resets itself for 2.5μs after the data valid pulse so the analog switch has a total of 7.5μs to settle down. This is more than adequate to assure that the A/D will ignore any switching transients.

For the circuit shown, the input voltage range is limited by the 4051 to ± 5 volts (V_{DD}, V_{EE}). If more input voltage range is needed, then V_{SS} and V_{EE} can be increased or the 1MΩ resistor can be replaced by individual resistors in front of each analog input. The exact value of each resistor is determined by dividing the maximum input voltage by 5μA. ($R_{IN} = V_{max} \div 5\mu A$).

The 950K and 100K resistor are used to provide an offset current of 5μA, allowing the analog input voltage to be negative as well as positive. If the input voltage does not go negative, then these two resistors can be deleted.

By adding additional 4051's, the number of analog inputs can be increased in multiples of eight. The additional binary outputs of the 4024 are then simply decoded to control the inhibit (1) input of each 4051.

If three-state outputs are needed for interfacing to a data buss, then the 8700 can be replaced by the 8703. The 8703 is identical to the 8700 except that the digital data outputs are three-state outputs controlled by pin 24 ($\overline{\text{ENABLE}}$).

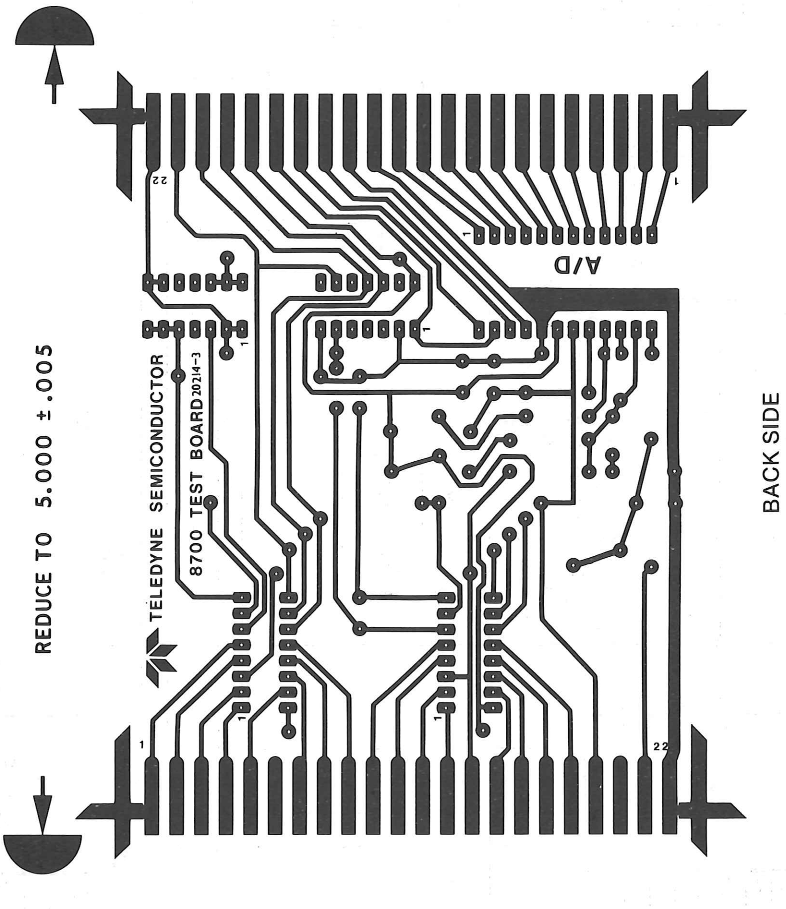


NOTES:

(1) Only one zero adjust control is required. For ± inputs use the 953K resistor and 100K potentiometer, ground pin 16 and delete the 1K, 100K and 20K components. When measuring only positive voltages delete the 953K resistor and the 100K potentiometer.

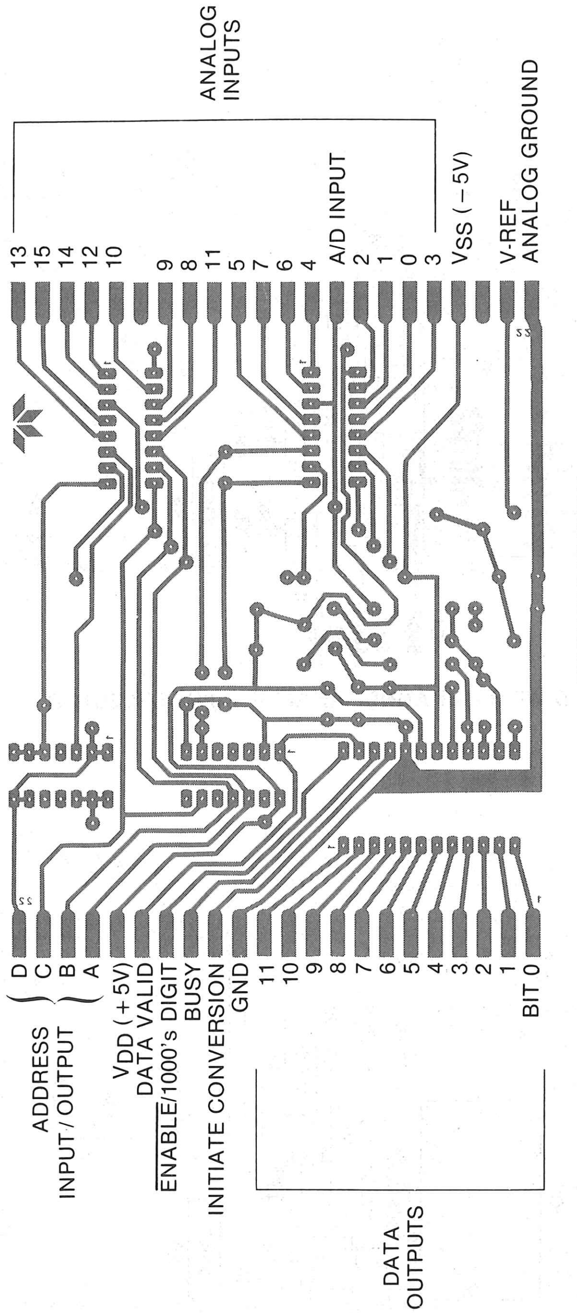
(2) For an eight channel data acquisition system ground this point and delete I_{C2} and I_{C5}.

8700 PC BOARD METAL PATTERN
PC BOARD FOR 1, 8, 16 CHANNEL DATA ACQUISITION SYSTEM



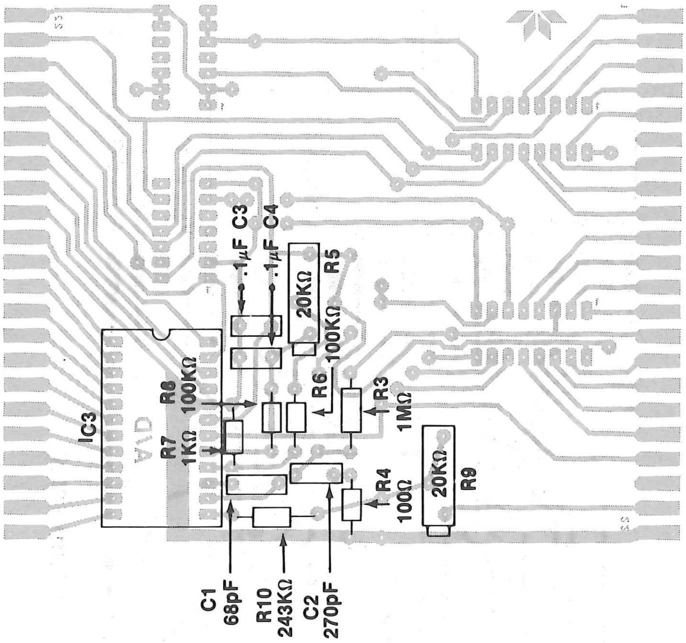
Note: PC board can be ordered from Teledyne as part #8700PC.

PIN-OUT DATA FOR 16 CHANNEL DATA ACQUISITION SYSTEM

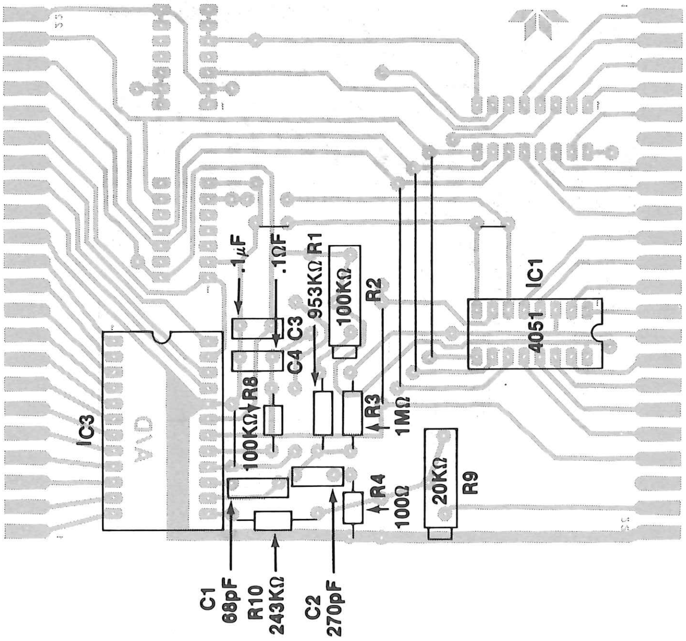


COMPONENT SIDE

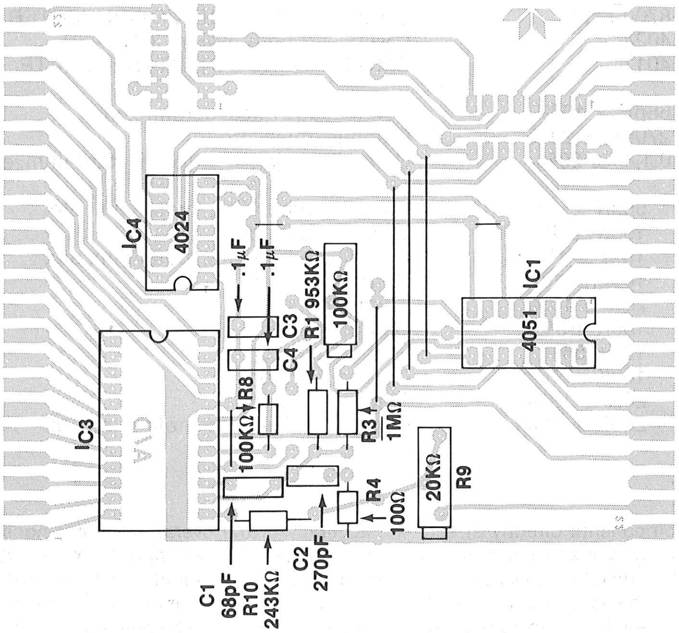
STANDARD TEST CIRCUIT



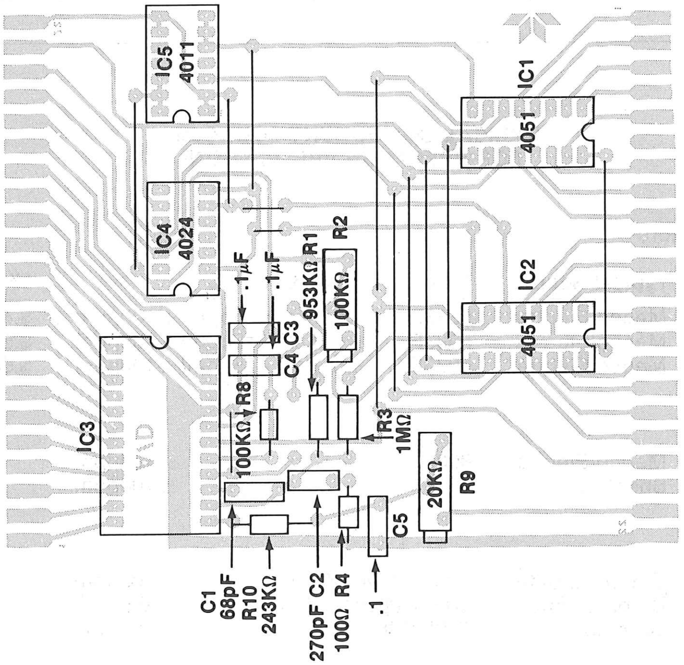
A/D WITH 8-CHANNEL ANALOG INPUT SELECTOR



8-CHANNEL DATA ACQUISITION SYSTEM



16-CHANNEL DATA ACQUISITION SYSTEM



PARTS LIST

16 CHANNEL DATA ACQUISITION SYSTEM

Ref #	Part Number	Description
IC1, IC2	4051	CMOS — 8 CHANNEL ANALOG SWITCH
IC3	8700 TYPE	CMOS — TELEDYNE A/D CONVERTER
IC4	4024	CMOS — 7 bit BINARY COUNTER
IC5	4011	CMOS — QUAD 2-INPUT NAND GATE
C1	68pF ± 10%	Low leakage mica, ceramic, etc.
C2	270pF ± 20%	Ceramic, mica, etc.
C3, C4, C5	0.1μF ± 20%	Ceramic, mylar, electrolytic, tantalum, etc.
R1	* 953K ± 1%	Carbon, carbon film, metal film, etc.
R2	* 100K ± 10%	Trimmer resistor
R3	* 1MΩ ± 1%	Carbon, carbon film, metal film, etc.
R4	100Ω ± 10%	Carbon resistor
R5	20K ± 10%	Trimmer resistor
R6	100K ± 5%	Carbon resistor
R7	1K ± 5%	Carbon resistor
R8	100K ± 10%	Carbon resistor
R9	* 20K ± 10%	Trimmer resistor
R10	* 243K ± 1%	Carbon, carbon film, metal film, etc.

★ The stability of these components directly affects the accuracy of the overall system. Choose components whose stability is consistent with the accuracy and temperature range required. For example, if an 8-bit A/D is used at a constant temperature, then 5% carbon resistors may be adequate since an 8-bit A/D's resolution is only 0.4%. However, if a 12-bit A/D (0.025% resolution) is to be used over the −55°C to + 125°C temperature range, then these components will be very critical and should have a stability of 5 to 15 ppm for fixed resistors and 25 to 50 ppm for variable resistors.

The following parts list of possible suppliers is intended to be of assistance in putting a converter design into production. It should not be interpreted as a comprehensive list of suppliers, nor does it constitute an endorsement by Teledyne Semiconductor.

TYPICAL COMPONENT SOURCES FOR PRECISION APPLICATION

A. Precision fixed resistors

Value	Tol.	Typical Source	Type	Temp. Coeff./°C	1K Price
243K	± 1%	Mepco/Electra	5033R	± 5ppm/ ± 25ppm/ ± 100ppm	$.41/$.26/$.10
953K	± 1%	Mepco/Electra	5033R	± 5ppm/ ± 25ppm/ ± 100ppm	$.58/$.40/$.16
1MΩ	± 1%	Mepco/Electra	5033R	± 5ppm/ ± 25ppm/ ± 100ppm	$.58/$.40/$.16

B. Variable resistors

20K/100K	± 10%	Mepco/Electra	8035	± 100ppm	$.63
20K/100K	± 10%	Spectrol	43P	± 100ppm	$.65

C. Capacitors

68pF	± 10%	Union Carbide	C114K680K1X1CA	± 800ppm	$.22
68pF	± 10%	Union Carbide	C114G680K565CM	± 30ppm	$.65
68pF	± 5%	Corning	CY06C680G	± 25ppm	$.80

1. AVOID INTRODUCING ERRORS:

Proper design procedures are necessary to obtain best accuracy from 8700 series converters.

a. Do not route logic signals under the 8700 or near any of the three analog terminals I_{IN}, I_{REF}, and Zero Adjust (pins 13, 14, 15, 16).

b. Plan your grounding. Keep the analog ground isolated from the logic ground by making the two electrically common only at the system ground.

c. Filter the supply voltages by using bypass capacitors of value 0.1μF or greater connected in shunt between the supply line and the logic ground (pin 20). Locate the capacitors as close as to the 8700 as practical.

d. Provide a reference as stable as the conversion accuracy you expect. Remember:

$$\text{DIGITAL COUNTS} = \frac{I_{IN}}{I_{REF}} \bullet A = \frac{V_{IN} \div R_{IN}}{V_{REF} \div R_{REF}} \bullet A$$

The conversion accuracy is a direct function of the V_{REF}. In terms of V_{REF} voltage regulation, the 8-bit requires ±.04%, the 10-bit, ±.01%, the 12-bit, ±.0025%, and the 3½ digit BCD, ±.005%,to introduce less than 1/10 LSB error.

e. Choose a full scale voltage range as large as possible; this will minimize the effect of zero drift and input noise. For example, a 50μV zero drift or noise voltage on the 8701 (10-bit) will produce a ± ½ LSB error at 500mV full scale, but only ± 1/40 LSB at 10V full scale.

2. OTHER SUGGESTIONS FOR IMPROVING PERFORMANCE:

a. For C_{INT}, virtually any type of non-polarized 68pF ±10% is acceptable. Locate as near to the converter as possible and away from noisy lines.

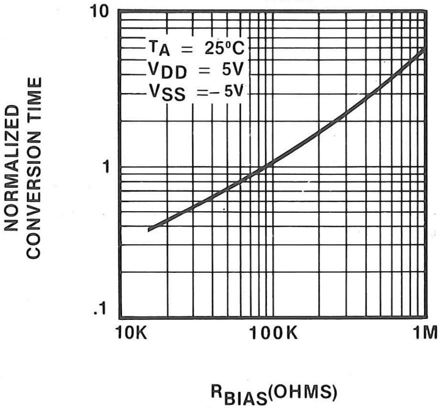
b. Locate R_{DAMP} and C_{DAMP} as near the converter as possible and away from noisy lines. The value of R_{DAMP} = 100Ω and C_{DAMP} = 270pF are nominal; these two elements stabilize the input op amp to prevent oscillations.

3. CAUTION: WHEN USING ZENERS, OP AMPS AND VOLTAGE REGULATORS:

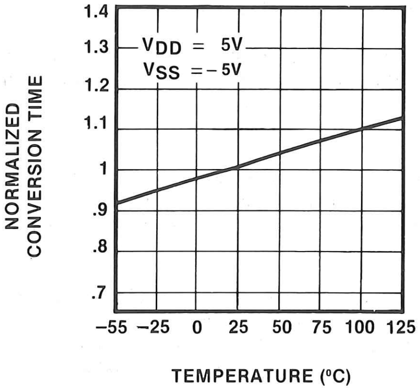
These devices are often used as input amplifiers, voltage references and power supplies for A/D converters. It is worth noting that these devices can generate quite a bit of "High Frequency" noise. Normally, this noise does not interfere with the operation of the A/D converter. However, excessive noise from zeners, used as voltage references for example, have been found to be the cause of strange counting sequences and non-linear A/D operation. It should therefore be standard practice to bypass all zeners and voltage regulators with at least 0.1μF capacitors. (If the zener is exceptionally noisy, 1 to 10μF capacitors may be required. Remember that zeners are often used as white noise sources in noise generators.)

If erratic operation is still observed, then either the op amp's feedback resistor or the output should be bypassed. Note also that the noise level of zeners, op amps and voltage regulators varies from lot to lot and especially from one manufacturer to another. Bypassing these devices during the design stage will prevent the noise level variation from becoming a possible production problem.

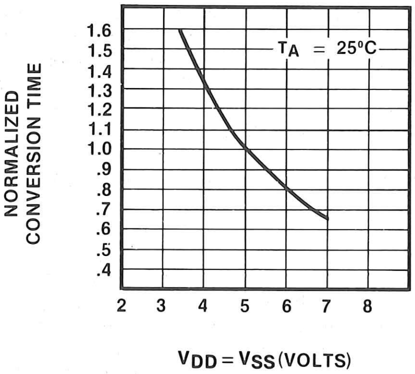
TYPICAL PERFORMANCE CURVES



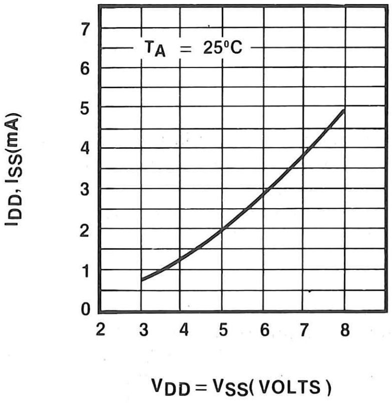
CONVERSION TIME vs R_{BIAS}



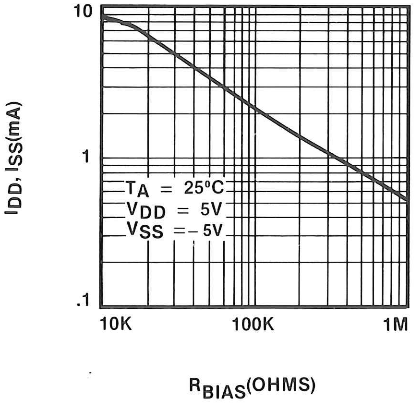
CONVERSION TIME vs TEMPERATURE



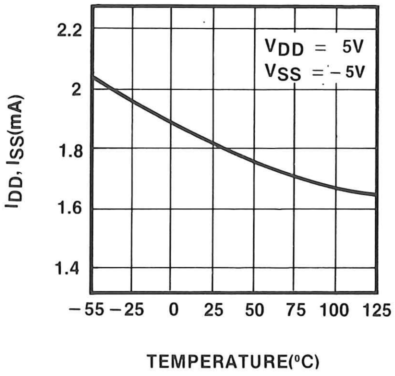
CONVERSION TIME vs SUPPLY VOLTAGE



SUPPLY CURRENT vs SUPPLY VOLTAGE



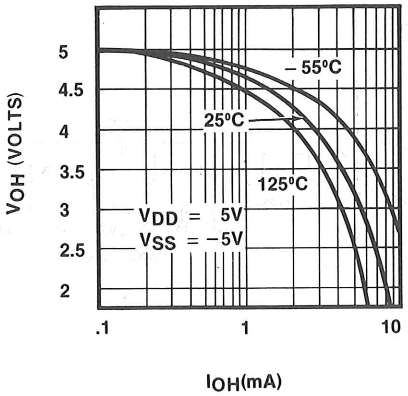
SUPPLY CURRENT vs R_{BIAS}



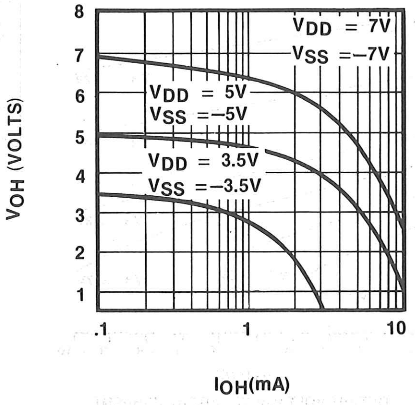
SUPPLY CURRENT vs TEMPERATURE

TYPICAL PERFORMANCE CURVES

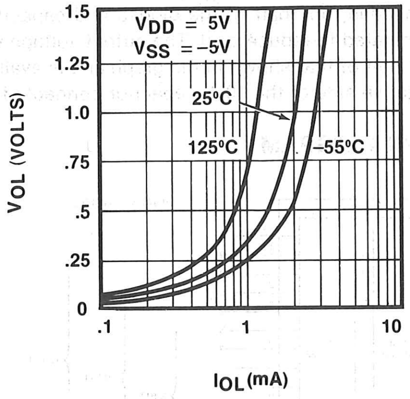
OUTPUT SOURCE CURRENT vs TEMPERATURE



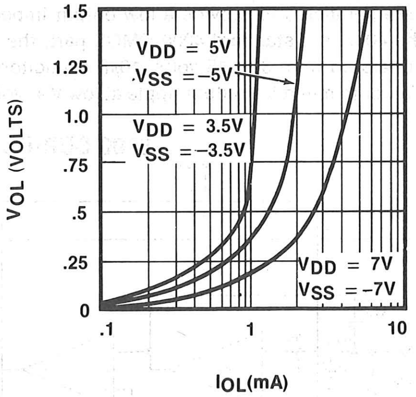
OUTPUT SOURCE CURRENT vs SUPPLY VOLTAGE



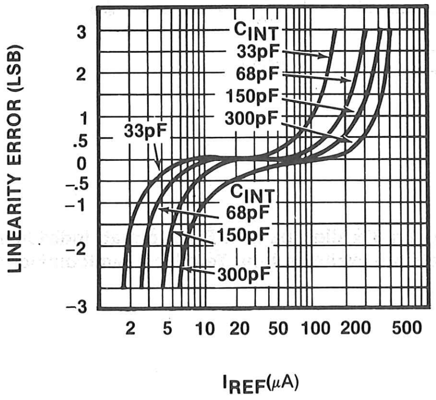
OUTPUT SINK CURRENT vs TEMPERATURE



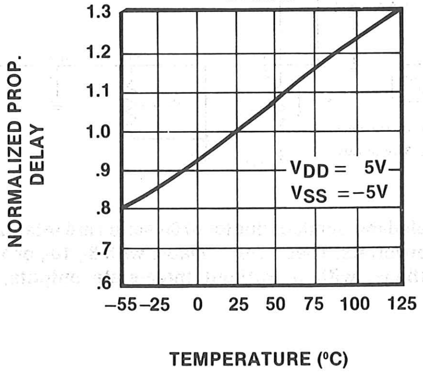
OUTPUT SINK CURRENT vs SUPPLY VOLTAGE



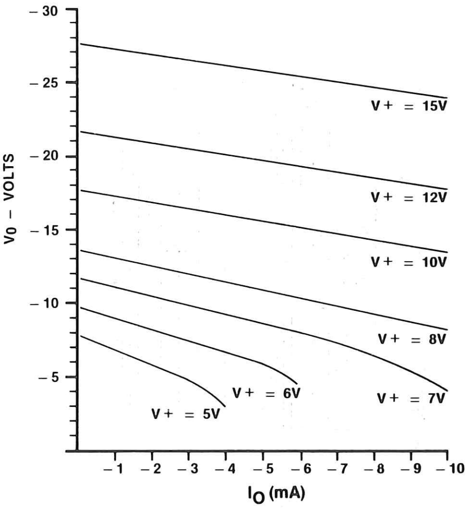
LINEARITY vs IREF



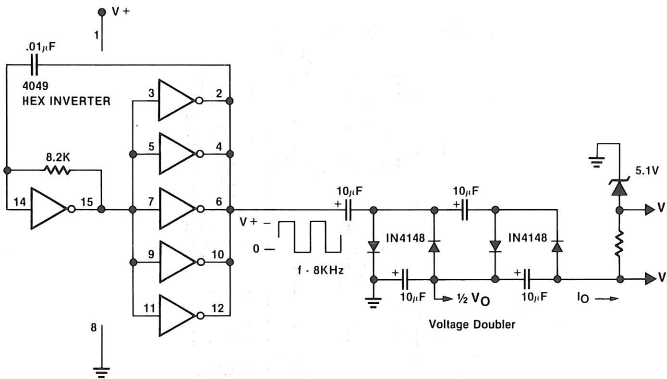
TRI-STATE PROPAGATION DELAY



NEGATIVE SUPPLY GENERATOR



OUTPUT VOLTAGE VS OUTPUT CURRENT

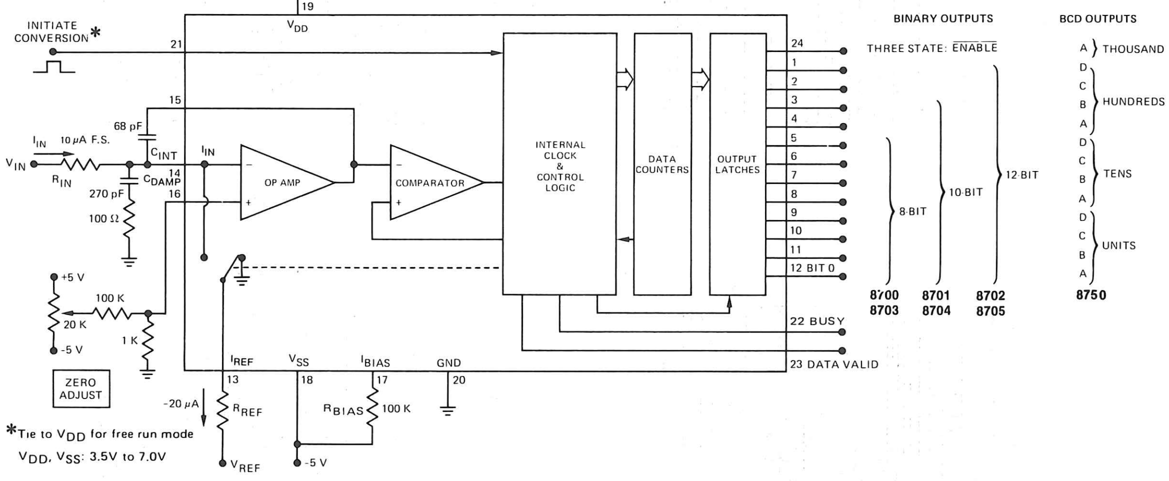


A negative voltage for V_{SS} and V_{REF} can be generated from the positive supply by using a hex inverter as a free running oscillator to drive a voltage doubler. The five inverters are paralleled to provide a low output impedance. Since the 4049 is a standard 4000 CMOS part, the circuit can be operated from 3 to 15 volts. 10μF capacitors were used in order to minimize output ripple at low V+ voltages.

When higher input voltages (V+) are available the 10μF capacitors can be lowered to 1 or 0.1μF depending on the output loading. If this circuit generates more voltage than is needed, one half of the diodes and capacitors can be eliminated to reduce cost. The output voltage will then be one half of that shown in the graph and is available on the negative side of the 10μF capacitor connected to ground.

8700 SERIES CONNECTION DIAGRAM

8700-8750



The Teledyne Semiconductor 8700 series are integrating A/D converters. These are available with 8-, 10-, or 12-bit resolutions, with or without three-state outputs, and also in a 3½ digit parallel BDC format. Individual data sheets are available from Teledyne Semiconductor.

III

Monolithic CMOS D/A Converters

Monolithic CMOS D/A Converters
8600 Series

8640, 8641
12-Bit Multiplying

Features

- 12 bit linearity (0.01% achieved without laser trimming)
- 2 ppm/°C max gain error tempco
- Full Four Quadrant Multiplication
- Low Power CMOS, <30mW
- TTL/CMOS Compatible Inputs
- Low feedthrough error
- Compensated feedback resistor
- Low cost
- 883B processing available
- Direct replacement for AD7521 and AD7541

Applications

- CRT Graphics Generator
- Synchro-to-digital converters
- Digitally controlled attenuators
- Programmable amplifiers
- Digitally controlled power supplies
- A/D Conversion
- Function Generators
- Digital Filters

Ordering Information

Temperature Range / Nonlinearity	0°C to +70°C	−25°C to +85°C	−55°C to +125°C
0.024%	8640CJ	8640CN	8640BN
0.012%	8641CJ	8641CN	8641BN

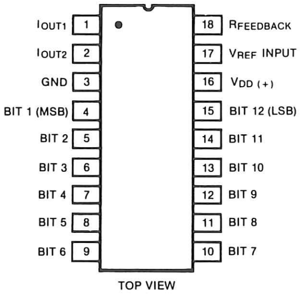
General Description

The 8640 and 8641 are 12-bit monolithic CMOS digital-to-analog converters featuring double layer metal interconnections for improved high speed operation and lower cost. The use of precision thin-film deposition resistors provides 12-bit linearity without laser trimming, thus eliminating any long-term instabilities laser trimming might introduce. The use of compensating FET switches in the feedback resistor and at the end of the ladder chain reduces gain error temperature coefficient to a maximum of 2 pm/°C.

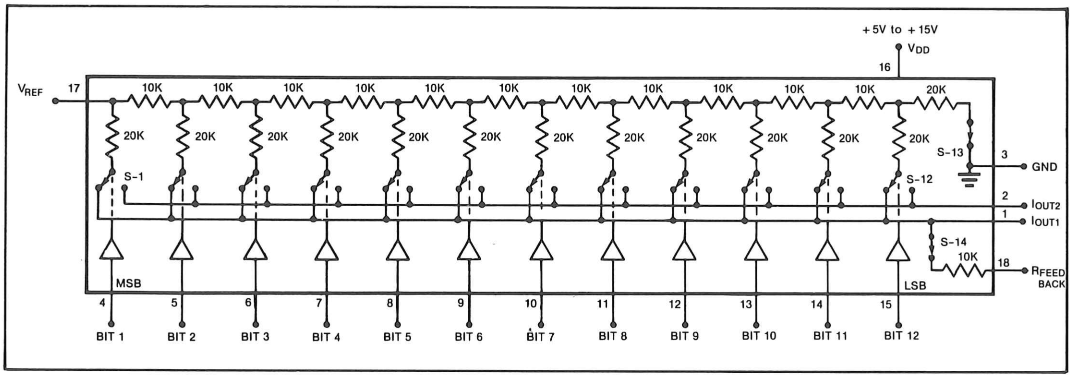
The 8640, 8641, 12-bit multiplying D/A converters consist of a highly stable thin film R-2R ladder and twelve CMOS current switches on a monolithic chip. Most applications require the addition of only an output operational amplifier and a voltage or current reference.

The 8640 and 8641 are pin for pin replacements for Analog Devices AD7541. They meet or exceed the performance of the AD7541, with improved supply rejection, lower variation of linearity and gain error with V_{DD}, and improved temperature stability.

Connection Diagram



Schematic Diagram



Absolute Maximum Ratings

($T_A = 25°$ unless otherwise noted)

Storage Temperature		−65°C to +150°C
Operating Temperature	CJ	0°C to −70°C
	CN	−25°C to +85°C
	BN	−55°C to −125°C
V_{DD} (to GND)		+17V
V_{REF} (to GND)		±25V
Digital Input Voltage Range		V_{DD} to GND
Output Voltage (Pin 1, Pin 2)		−100mV to V_{DD}
Package Dissipation Derate above +75°C by		450mW 6mW
Lead Temperature (Soldering, 10 seconds)		300°C

CAUTION

1. Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF}.
2. The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic field. Terminate all unused inputs. Store in conductive foam at all times. Use proper anti-static handling procedures.

Electrical Characteristics

NOTE: Unless otherwise specified, V_{DD} = +15V, V_{REF} = +10V. See page 7 for definitions and test circuits.

	T_A = 25°C			T_A = Full Temp Range				
PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS	CONDITIONS
STATIC ACCURACY								
Resolution	12			12			bits	
Nonlinearity 8640			±1			±1	LSB	V_{OUT1} = V_{OUT2} = 0V
8641			± ½			± ½	LSB	V_{OUT1} = V_{OUT2} = 0V
Nonlinearity Tempco			2			2	ppm/°C	
Gain Error[2]			±0.3				%FSR[1]	
Gain Error Tempco			2			2	ppm/°C	
Power Supply Sensitivity			0.003			0.005	%per%	V_{DD} = 15V ± 0.5V
Output Leakage Current			±50			±200	nA	V_{REF} = ±10V
DYNAMIC PERFORMANCE								
Output Current Settling Time			500			500	nS	to 2 LSB (.05%)
			1			1	µS	to ½ LSB (.01%)
Feedthrough Error			1			1	mVpp	V_{REF} = 20Vpp @ 10 kHz
REFERENCE INPUT								
Input Resistance	5	10	20	5		20	kΩ	
DIGITAL INPUTS								
V_{INH}			2.4			2.4	V	
V_{INL}	0.8			0.8			V	
Input Leakage Current			±1			±1	µA	V_{IN} = 0 or 15V
Input Capacitance			8			8	pF	
ANALOG OUTPUT CAPACITANCE								
C_{OUT1}			200			200	pF	Digital Inputs = V_{INH}
C_{OUT2}			60			60	pF	Digital Inputs = V_{INH}
C_{OUT1}			60			60	pF	Digital Inputs = V_{INL}
C_{OUT2}			200			200	pF	Digital Inputs = V_{INL}
POWER REQUIREMENTS								
V_{DD}Range	5		16	5		16	V	Accuracy is not guaranteed over this range
I_{DD}			2			2	mA	Digital Inputs = V_{INH} or V_{INL}

NOTES: 1. FSR is Full Scale Range
2. Using internal feedback resistor.

Typical Performance Characteristics

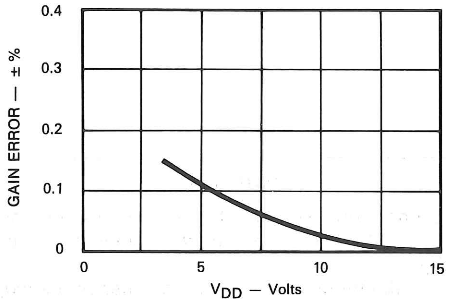


Figure 1. Gain Error vs. Supply Voltage

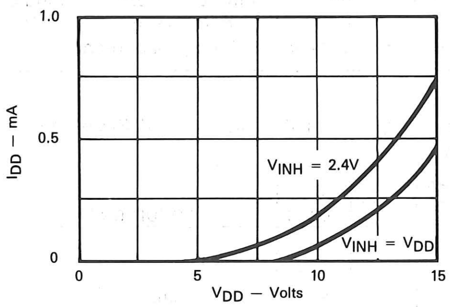


Figure 2. Supply Current vs. Supply Voltage

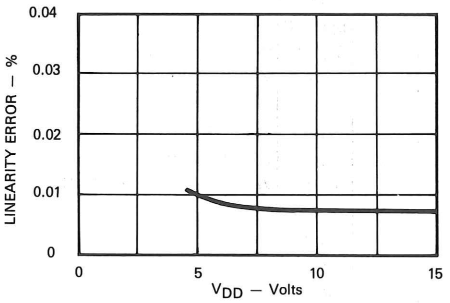


Figure 3. Linearity Error vs. Supply Voltage

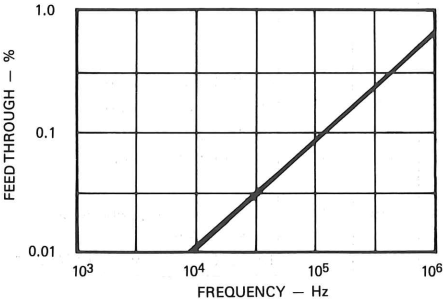


Figure 4. Feedthrough Error vs. Frequency

Application Hints

Linearity depends on the voltage at I_{OUT1} and I_{OUT2} (pin 1 and pin 2) being exactly equal to GND (pin 3) and to the output amplifier's non-inverting (+) input. Careful PC board layout and adjustment and selection of the amplifier's offset voltage and bias current are necessary.

The input structures of some high speed operational amplifiers can attempt to draw substantial current during switch-on. Schottky diodes should be used in these circumstances to prevent exceeding the absolute maximum rating for V_{OUT1} and V_{OUT2}.

The power supply should be carefully checked for noise, which would affect performance, and overshoot which could damage the device.

Unused digital inputs must always be grounded or tied to V_{DD} to ensure correct operation. Particular care should be taken when digital inputs are routed to another PC card. It is recommended that inputs open-circuited when PC cards are disconnected be taken to V_{DD} or GND via high value (1MΩ) resistors to prevent the buildup of static charge.

Circuit Description

The 8640, 8641, 12-bit multiplying D/A converters consist of a highly stable thin film R-2R ladder and twelve CMOS current switches on a monolithic chip. Most applications require the addition of only an output operational amplifier and a voltage or current reference.

The simplified D/A circuit is shown in Figure 5. An inverted R-2R ladder structure is used—that is, the binarily weighted currents are switched between the I_{OUT1} and the I_{OUT2} bus lines thus maintaining a constant current in each ladder leg independent of the switch state.

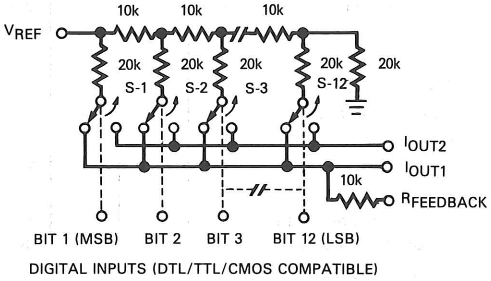


Figure 5. D/A Functional Diagram
(Inputs "HIGH")

One of the CMOS current switches is shown in Figure 6. The geometries of devices 1, 2 and 3 are optimized to make the digital control inputs DTL/TTL/CMOS compatible over the full military temperature range. The input stage drives two inverters (devices 4, 5, 6 and 7) which in turn drive the two output N-channels. The "ON" resistances of the switches are binarily scaled so the voltage drop across each switch is the same. For example, switch 1 of Figure 5 was designed for an

"ON" resistance of 10 ohms, switch 2 of 20 ohms and so on. For a 10V reference input, the current through switch 1 is 0.5mA, the current through switch 2 is 0.25mA, and so on, thus maintaining a constant 5mV drop across each switch. It is essential that each switch voltage drop be equal if the binarily weighted current division property of the ladder is to be maintained.

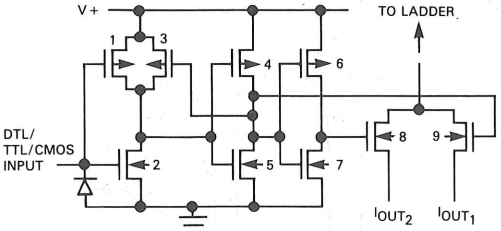


Figure 6. CMOS Switch

Equivalent Circuit Analysis

The equivalent circuits for all digital inputs high and all digital inputs low are shown in Figures 7 and 8. In Figure 7 with all digital inputs low, the reference current is switched to I_{OUT2}. The current source $I_{LEAKAGE}$ is composed of surface and junction leakages to the substrate while the 1/4096 current source represents a constant 1-bit current drain through the termination resistor on the R-2R ladder. The "ON" capacitance of the output N-channel switch is 200pF, as shown on the I_{OUT2} terminal. Analysis of the circuit for all digital inputs high, as shown in Figure 8, is similar to Figure 7; however, the "ON" switches are now on terminal I_{OUT1}, hence the 200pF at that terminal.

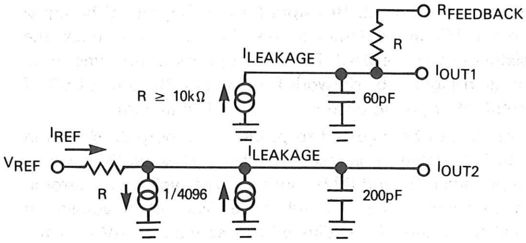


Figure 7. DIA Equivalent Circuit —
All Digital Inputs Low

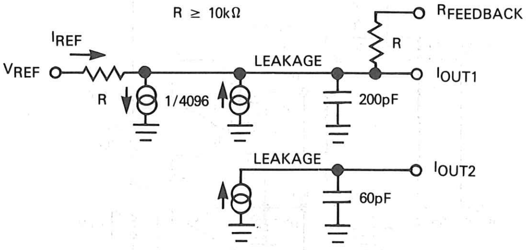


Figure 8. DIA Equivalent Circuit —
All Digital Inputs High

Dynamic Performance

Output Impedance

The preceding circuit analysis shows that the output capacitance is dependent upon the digital code, as is the output resistance. Looking back into I_{OUT1} the resistance varies between 10kΩ ($R_{FEEDBACK}$ alone) and 5kΩ (R_F in parallel with the 10kΩ network resistance.)

This variation affects both static accuracy and dynamic performance. The effect on static accuracy is further considered on pages 5 and 6. The dynamic performance of the D/A will depend upon the gain and phase stability of the output amplifier, together with the optimum choice of PC board layout and decoupling components.

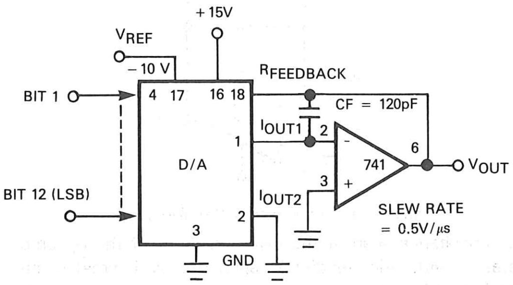


Figure 9. DAC Circuit Using 741 Op Amp

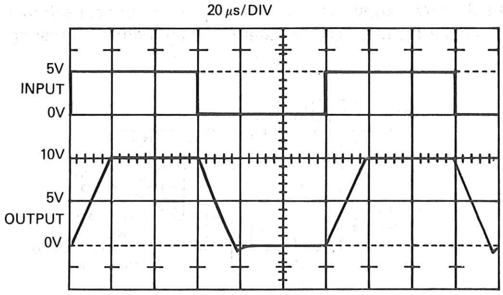


Figure 10. Output Waveform with 741 Op Amp

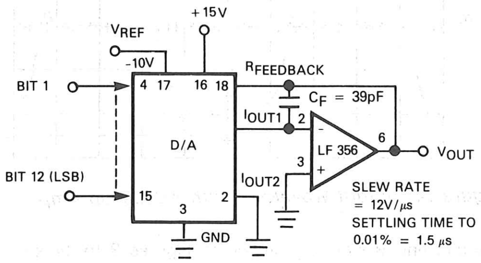


Figure 11. DAC Circuit Using LF356 Op Amp

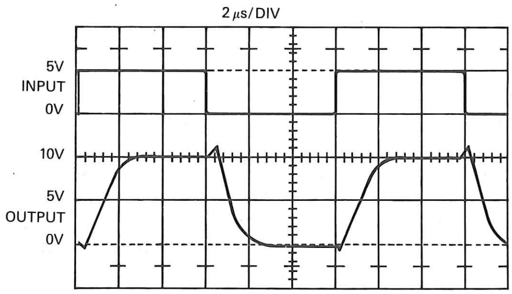


Figure 12. Output Waveform with LF 356 Op Amp

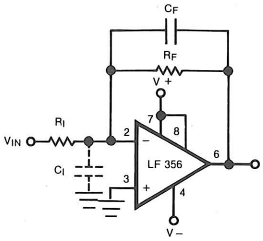


Figure 12A. Optimizing Settling Time

The capacitance seen at the inverting input of the op amp interacts with the feedback elements and creates an undesirable high frequency pole. In order to optimize the settling time and step response of the entire D/A system, a compensation capacitor, C_F, needs to be added such that $R_IC_I \cong R_FC_F$. C_I is equal to the sum of the op amp input capacitance plus the D/A output capacitance and the layout capacitance. The final value of C_F is best determined by actual lab testing.

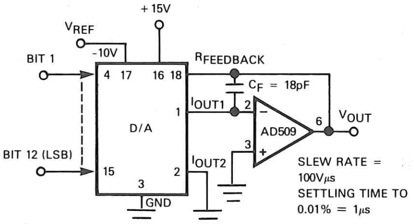


Figure 13. DAC Circuit Using AD509

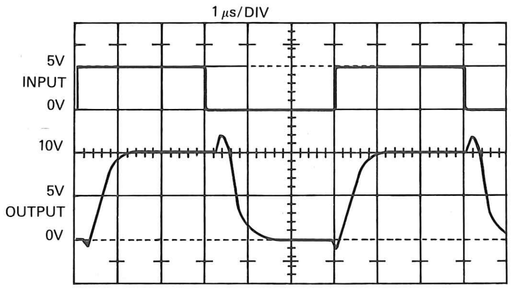


Figure 14. Output Waveform with AD509 Op Amp

The circuits and waveforms shown in Figures 9 to 14 are representative of the three principal types of output amplifiers: a general purpose low drift (741), a fast settling, high speed, low cost op amp (LF 356), and a fast settling unit (AD509).

Points to remember when applying high speed amplifiers include:

1. Protection diodes as shown in Figures 15 and 16.
2. Phase compensation for the DAC's output capacitance (C_F).
3. Power supply decoupling and correct grounding.

Applications

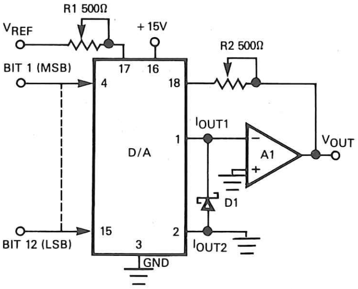


Figure 15. Unipolar Binary Operation

Unipolar Binary Operation

The connections required for unipolar digital binary operation are shown above. V_{REF} may be positive or negative so 2-quadrant multiplication may be performed. Schottky diode D1 (HP5082-2811, IN5817, MBR120P or equivalent) protects I_{OUT1} from negative excursions which could damage the device. This precaution is only necessary with certain high speed amplifiers.

Bipolar (4-Quadrant) Binary Operation

The digital input is offset binary coded and multiplies V_{REF} according to Table 2. Resistors R1 and R2 should be equal within 0.1% at all temperatures, but need not track the resistors within the DAC. D1 and D2 perform the same function as in Figure 15. Network R3, R4 and R5 sum ½LSB of current into I_{OUT2} to ensure correct coding at zero.

R1 or R2 can be adjusted to produce the outputs shown in Table 1. However, it is recommended that when the application permits it R1 and R2 be omitted. The typical gain error in this condition is 0.3% of full scale. The offset voltage of amplifier A1 should be adjusted to less than 0.5mV over the temperature range.

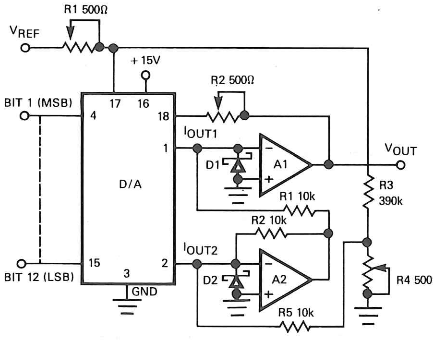


Figure 16. Bipolar (4-Quadrant) Binary Operation

Digital Input	Nominal Analog Output
1 1 1 1 1 1 1 1 1 1 1 1	$-0.99975\ V_{REF}$
1 0 0 0 0 0 0 0 0 0 0 0	$-0.50000\ V_{REF}$
0 1 0 0 0 0 0 0 0 0 0 0	$-0.25000\ V_{REF}$
0 0 0 0 0 0 0 0 0 0 0 0	0

Table 1. Code Table for Unipolar Operation (Figure 15)

Digital Input	Nominal Analog Output
1 1 1 1 1 1 1 1 1 1 1 1	$-0.99951\ V_{REF}$
1 0 0 0 0 0 0 0 0 0 0 1	$-0.00049\ V_{REF}$
1 0 0 0 0 0 0 0 0 0 0 0	0
0 1 0 0 0 0 0 0 0 0 0 0	$+0.50000\ V_{REF}$
0 0 0 0 0 0 0 0 0 0 0 0	$+1.00000\ V_{REF}$

Table 2. Code Table for Bipolar Operation (Figure 16)

Amplifiers A1 and A2 should be adjusted to an input offset of less than 0.1mV and should be better than 0.5mV over the temperature range. With V_{REF} set to approximately 10V, R4 should be adjusted so that with code 100000000000 V_{OUT} = 0V ±0.2mV. R1 or R2 should be adjusted so that with code 000000000000 $V_{OUT} = V_{REF}$.

As with the unipolar circuit R1 and R2 can be omitted, with a resulting typical gain error of 0.3% of full scale. R4 may be replaced by a 100Ω fixed resistor. In this case, the typical zero error is 0.015% of F.S.R.

Output Amplifier Considerations

It has already been pointed out that the DAC output resistance varies with the digital code. The effect this has on static accuracy will now be considered.

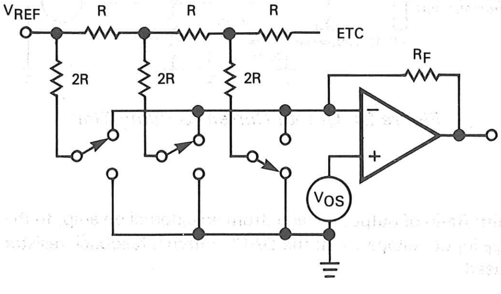


Figure 17. Output Amplifier

$$\text{The error voltage} = V_{OS}\left(1 + \frac{R_F}{R_O}\right)$$

R_O is a function of the digital code.
R_O ≅ 10kΩ for any more than 4-bits Logic 1.
R_O ≅ 30kΩ for any single bit Logic 1.

The gain for offset, therefore, changes as follows:

$$\text{At code 001111111111 } V_{ERROR1} = V_{OS}\left(1 + \frac{10k}{10k}\right) = 2\ V_{OS}$$

$$\text{At code 010000000000 } V_{ERROR2} = V_{OS}\left(1 + \frac{10k}{30k}\right) = \frac{4}{3}\ V_{OS}$$

The error difference is therefore $\frac{2}{3}\ V_{OS}$.

Since, for a 12-bit resolution DAC, one LSB has a weight (for V_{REF} = 10V) of 2.5mV, it is clearly important that V_{OS} be nulled, either using the amplifier's nulling facility or an external network.

It is important to realize that an offset can be caused by including the usual bias current compensation resistor in the amplifier's non-inverting input terminal. This should not be used. Instead the amplifier should have a bias current which is low over the temperature range of interest, and should certainly not exceed 75nA.

Analog/Digital Division

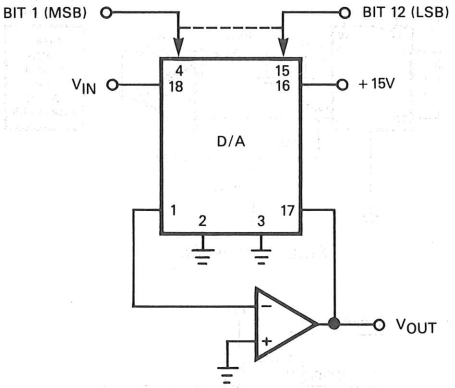


Figure 18. Analog/Digital Divider

With the D/A connected in its normal multiplying configuration shown in Figure 15, the transfer function is

$$V_O = -V_{IN}\left(\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \ldots.\ \frac{A_{12}}{A^{12}}\right)$$

where the coefficients A_X assume a value of 1 for an ON bit and 0 for an OFF bit.

By connecting the DAC in the feedback of an operational amplifier, as shown in Figure 18, the transfer function becomes

$$V_O = \left(\frac{-V_{IN}}{\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \ldots.\ \frac{A_{12}}{2^{12}}}\right)$$

This is division of an analog variable (V_{IN}) by a digital word. With all bits off, the amplifier output goes to the supply rails since division by zero is not defined. With the LSB (Bit 12) ON, the gain is 4096. With all bits ON, the gain is 1 (±1LSB).

Test Circuits

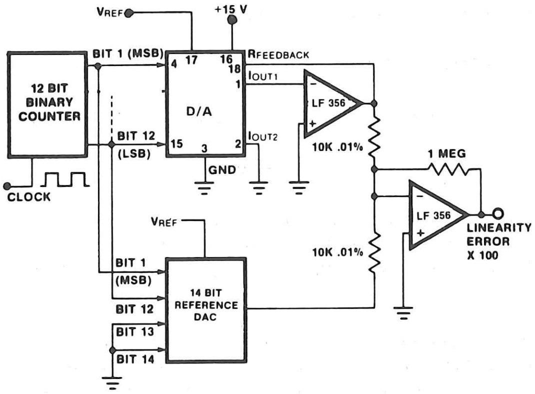


Figure 19. Nonlinearity

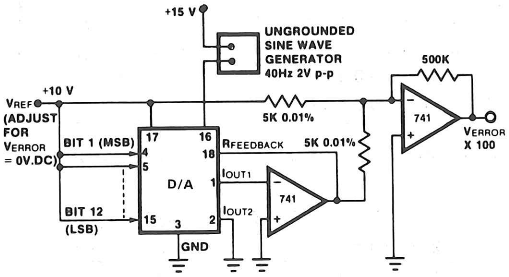


Figure 22. Power Supply Rejection

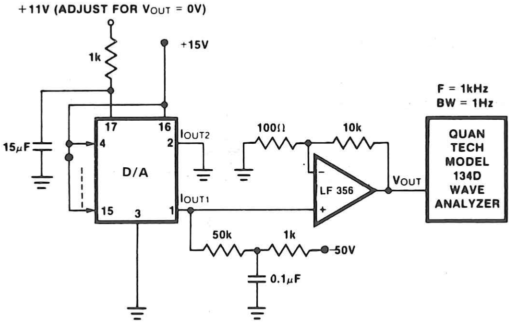


Figure 20. Noise

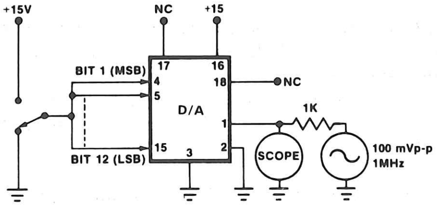


Figure 23. Output Capacitance

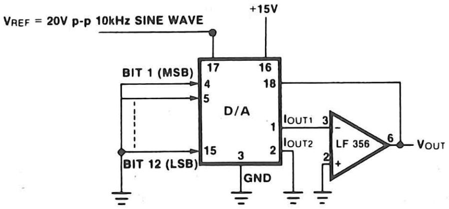


Figure 21. Feedthrough Error

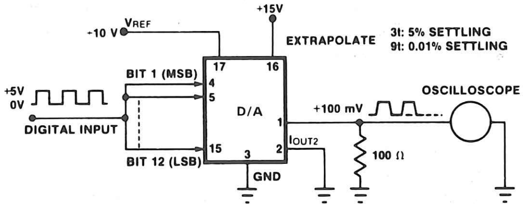


Figure 24. Output Current Settling Time

Specification Definitions

Nonlinearity: Error caused by deviation of the DAC transfer function from a best straight line fit. Normally expressed as a percentage of full scale. For a multiplying DAC, this should hold true over the entire V_{REF} range.

Resolution: Value of the LSB. For example, a unipolar converter with n bits has a resolution of (2^{-n}) (V_{REF}). A bipolar converter of n bits has a resolution of $[2^{-(n-1)}]$ $[V_{REF}]$. Resolution in no way implies linearity.

Settling Time: Time required for the output of the DAC to settle to within ½ LSB for a given digital input change, i.e., 0 to Full Scale.

Gain: Ratio of output voltage, from an external op amp, to the V_{REF} input voltage when the DAC's internal feedback resistor is used.

Feedthrough Error: Error caused by capacitive coupling from V_{REF} to the output with all switches OFF.

Output Capacitance: Capacity from I_{OUT1} and I_{OUT2} to ground.

Output Leakage Current: Current which appears on I_{OUT1} terminal with all digital inputs LOW or on I_{OUT2} terminal when all inputs are HIGH.

Digital/Synchro Converter

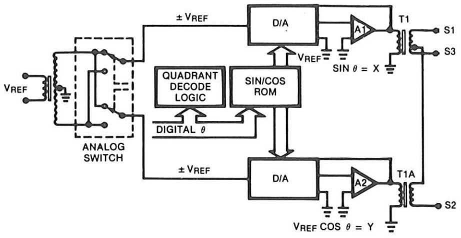


Figure 25. 14-Bit Digital to Synchro Converter

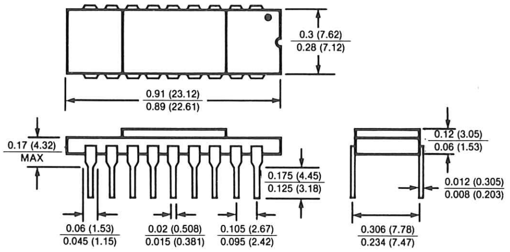
The low cost and high accuracy available from the Teledyne Semiconductor 8640, 8641 together with their bipolar multiplying capability, are exploited fully in the circuit of Figure 25. V_{REF} is normally 400Hz but by replacing the transformers with dc-coupled circuits coordinate transformation may be performed.

The SIN/COS ROM is readily available at low cost and the Analog switch enables greater resolution to be obtained.

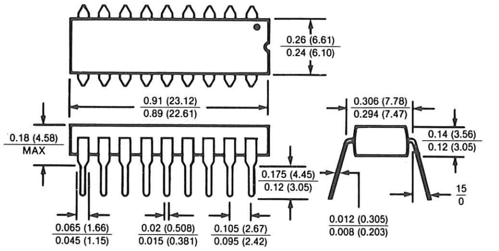
Resolver-to-synchro transformation is performed by the Scott connected pair T1 and T1A. The power available to the load connected to S1, S2 and S3 is determined by the amplifiers A1 and A2. A particular advantage of the circuit shown in Figure 19 is that it is invariant with respect to θ, and may be used to directly drive equipment such as CRT displays.

Physical Dimensions

Dimensions shown in inches and (mm).



N Package
18-Pin Ceramic DIP



J Package
18-Pin Plastic DIP

NOTE: Pin 1 indicated by adjacent dot, indent or end notch.

IV

Voltage to Frequency and Frequency to Voltage Converters

Voltage to Frequency Frequency to Voltage Converters

9400
9401
9402

Features

Voltage-to-Frequency

1Hz to 100kHz Operation

Choice of Guaranteed Linearity:

9401	.01%
9400	.05%
9402	.25%

±25ppm/°C Typ. Gain Temperature Stability

Open Collector Output

Output can Interface with any Form of Logic

Pulse and Square Wave Outputs

Programmable Scale Factor

Low Power Dissipation (27mW Typ.)

Single Supply Operation (8V to 15V)

Dual Supply Operation (±4V to ±7.5V)

Current or Voltage Input

Frequency-to-Voltage

DC to 100kHz Operation

Choice of Guaranteed Linearity:

9401	0.02%
9400	0.05%
9402	0.25%

Op Amp Output

Programmable Scale Factor

High Input Impedance (>10MΩ)

Accepts any Voltage Wave Shape

General Description

The Teledyne 9400 Series are low cost Voltage-to-Frequency converters combining Bipolar and CMOS technology on the same substrate. The converters accept a variable analog input signal and generate an output pulse train whose frequency is linearly proportional to the input voltage.

The 9400 Series can also be used as highly accurate Frequency-to-Voltage converters, accepting virtually any input frequency waveform and providing a linearly proportional voltage output.

A complete V/F or F/V system requires the addition of two capacitors and three resistors and reference voltage. In addition the 9400's operate on single or dual supply voltages.

Ordering Information

9400 CJ	14 Pin Plastic DIP (0°C to 70°C)
9401 CJ	14 Pin Plastic DIP (0°C to 70°C)
9402 CJ	14 Pin Plastic DIP (0°C to 70°C)
9400 CN	14 Pin Ceramic DIP (-40°C to +85°C)
9401 CN	14 Pin Ceramic DIP (-40°C to +85°C)

Applications

Voltage-to-Frequency

Temperature Sensing and Control

μP Data Acquisition

Instrumentation

13-Bit A/D Converters

Digital Panel Meters

Analog Data Transmission and Recording

Phase Locked Loops

Medical Isolation

Transducer Encoding

Alternate to 555 Astable Timer

Frequency-to-Voltage

Frequency Meters/Tachometer

Speedometers

Analog Data Transmission and Recording

Medical Isolation

Motor Control

RPM Indicator

FM Demodulation

Frequency Multiplier/Divider

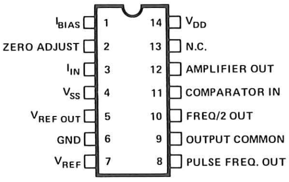
Flow Measurement and Control

Absolute Maximum Ratings

Storage Temperature		-65°C to +150°C
Operating Temperature	(J Package)	0°C to 70°C
	(N Package)	-40°C to +85°C
$V_{DD} - V_{SS}$		18V
I_{IN}		10mA
V_{OUT} Max — V_{OUT} Common		25V
$V_{REF} - V_{SS}$		-1.5V
Package Dissipation		500mW
Lead Temperature (Soldering, 10 sec)		300°C

HANDLING PRECAUTIONS: The 9400 Series are CMOS Bipolar devices and must be handled correctly to prevent damage. Package and store only in conductive foam, anti-static tubes or other conductive material. Use proper anti-static handling procedures. Do not connect in circuits under "power on" conditions, as high transients may cause permanent damage.

Connection Diagram



NOTE: PIN 1 INDICATED BY ADJACENT DOT (N PACKAGE), INDENT OR END NOTCH (J PACKAGE).

Electrical Characteristics, V/F Mode

Unless otherwise specified, V_{DD} = +5V, V_{SS} = —5V, V_{GND} = 0, V_{REF} = —5V, R_{BIAS} = 100KΩ, Full Scale = 10KHz. T_A = 25°C unless Full Temp. Range is specified (—40°C to +85°C for N package, 0°C to 70°C for J package).

VOLTAGE-TO-FREQUENCY		**9401**			**9400**			**9402**				
Parameter	**Definition**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Units**	**Notes**
Accuracy Linearity (10KHz)	Output Deviation from Straight Line between Normalized Zero and Full Scale Input		0.004	**0.01**		0.01	**0.05**		0.05	**0.25**	% Full Scale	
Linearity (100KHz)			0.04	0.08		0.1	0.25		0.25	0.50	% Full Scale	
Gain Temperature Drift	Variation in Gain (A) due to Temperature Change		±25	±40		±25	±40		±50	±100	ppm/°C Full Scale	1
Gain Variance	Variation from Exact A (Compensate by Trimming R_{IN}, V_{REF}, or C_{REF})		±10			±10			±10		% of Nominal	
Zero Offset	Correction at Zero Adjust for Zero Output When Input is Zero		±10	±50		±10	±50		±20	±100	mV	2
Zero Temperature Drift	Variation in Zero Offset Due to Temperature Change		±25	±50		±25	±50		±50	±100	μV/°C	1
Analog Inputs I_{IN} Full Scale	Full Scale Analog Input Current to Achieve Specified Accuracy		10			10			10		μA	
I_{IN} Overrange	Overrange Current			50			50			50	μA	
Response Time	Settling Time to 0.01% Full Scale		2			2			2		Cycles	
Digital Outputs V_{SAT} @ I_{OL}=10μA	Logical "0" Output Voltage			0.4			0.4			0.4	V	3
V_{OUT} Max. — V_{OUT} Common	Voltage Range between Output and Common			18.0			18.0			18.0	V	4
Pulse Frequency Output Width			3.0			3.0			3.0		μsec	
Supply Current I_{DD} Quiescent	Current Required from Positive Supply During Operation											
(N Package)			2.0	4.0		2.0	4.0				mA	9
(J Package)			2.0	6.0		2.0	6.0		3.0	10.0	mA	
I_{SS} Quiescent	Current Required from Negative Supply During Operation											
(N Package)			-1.5	-4.0		-1.5	-4.0				mA	10
(J Package)			-1.5	-6.0		-1.5	-6.0		-3.0	-10.0	mA	
V_{DD} Supply	Operating Range of Positive Supply	4.0		7.5	4.0		7.5	4.0		7.5	V	
V_{SS} Supply	Operating Range of Negative Supply	-4.0		-7.5	-4.0		-7.5	-4.0		-7.5	V	
Reference Voltage V_{REF}—V_{SS}	Range of Voltage Reference Input	-1.0			-1.0			-1.0			V	

NOTES:

1. Full temperature range.
2. I_{IN} = 0.
3. Full temperature range, I_{OUT} = 10mA.
4. I_{OUT} = 10μA.
5. 10Hz to 100KHz.
6. 5μs min. positive pulse width and 0.5μs min. negative pulse width.
7. T_r = t_f = 20ns.
8. R_L ≥ 2KΩ.
9. Full temperature range, V_{IN} = -0.1V.
10. V_{IN} = -0.1V.
11. I_{IN} connects the summing junction of an operational amplifier. Voltage sources cannot be attached directly but must be buffered by external resistors.

V/F Circuit Description

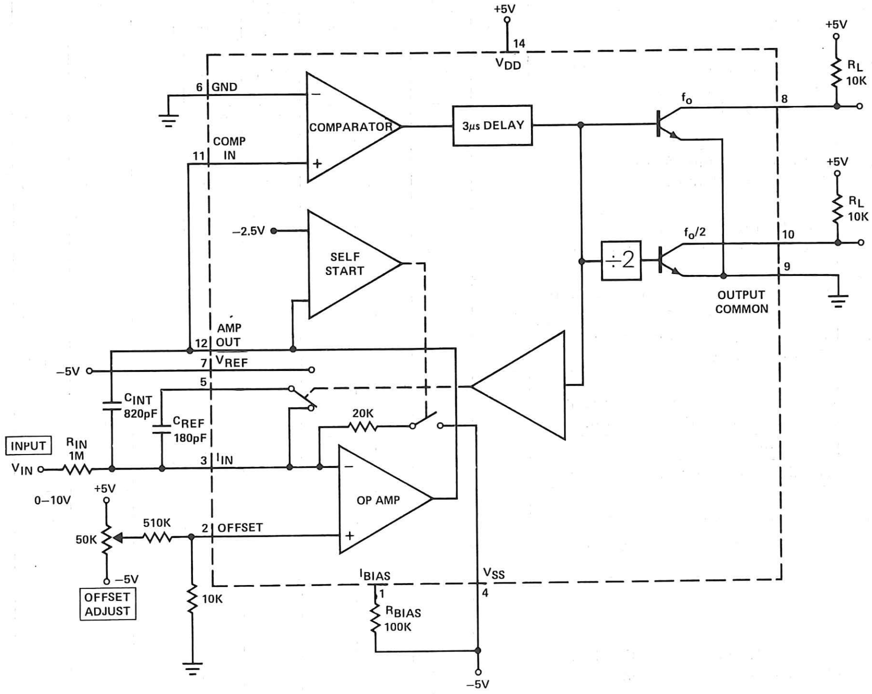
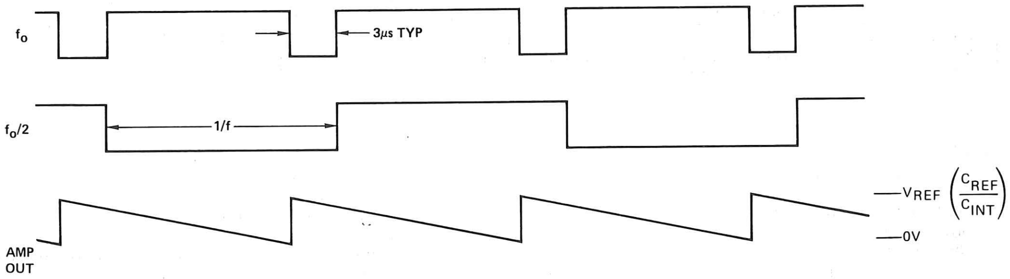


Figure 1. 10Hz to 10KHz V/F Converter



1. To adjust f_{min}, set V_{IN}=10mV and adjust the 50K offset for 10Hz out.
2. To adjust f_{max}, set V_{IN} =10V and adjust R_{IN} or V_{REF} for 10KHz out.
3. To increase f_{OUT}MAX to 100KHz change C_{REF} to 27pF and C_{INT} to 75pF.
4. For high performance applications use high stability components for R_{IN}, C_{REF}, V_{REF} (metal film resistors and glass film capacitors). Also separate the output ground (Pin 9) from the input ground (Pin 6).

Figure 2. Output Waveforms

V/F Circuit Description (Contd.)

The Teledyne 9400 V/F Converter operates on the principal of charge balancing. The input voltage (V_{IN}) is converted to a current (I_{IN}) by the input resistor. This current is then converted to a charge by the integrating capacitor and shows up as a linearly decreasing voltage at the output of the op amp. The zero crossing of the output is sensed by the comparator causing the reference voltage to be applied to the reference capacitor for a time period long enough to virtually charge the capacitor to the reference voltage. This action reduces the charge on the integrating capacitor by a fixed amount ($q = C_{REF} \times V_{REF}$) causing the op amp output to step up a finite amount.

At the end of the charging period, C_{REF} is shorted out dissipating the stored reference charge so that when the output again crosses zero, the system is ready to recycle. In this manner, the continued discharging of the integrating capacitor by the input is balanced out by fixed charges from the reference voltage. As the input voltage is increased, the number of reference pulses required to maintain balance increases causing the output frequency to also increase. Since each charge increment is fixed the increase in frequency with voltage is linear. In addition, the accuracy of the output pulses does not directly effect the linearity of the V/F. It must simply be long enough for full charge transfer to take place.

The 9400 contains a "self-start" circuit to assure that the V/F will always operate properly when power is first applied. In the event that during "Power-on" the op amp output is below the comparator threshold and C_{REF} is already charged, a positive voltage step will not occur. The op amp output will continue to decrease until it crosses the −2.5 volt threshold of the "self-start" comparator. When this happens a resistor is connected to the op amp input causing the output to quickly go positive until the 9400 is once again in its normal operating mode.

The 9400 utilizes both bipolar and MOS transistors on the same substrate, taking advantage of the best features of each. MOS transistors are used at the inputs to reduce offset and bias currents. Bipolar transistors are used in the op amp, for high gain, and on all outputs for excellent current driving capabilities. CMOS logic is used throughout to minimize power consumption.

Pin Functions

Comparator Input — In the V/F mode, this input is connected to the amplifier output (pin 12) and triggers the 3μsec pulse delay when the input voltage passes its threshold. In the F/V mode, the input frequency is applied to the comparator input.

Pulse Freq Out — This output is an open-collector bipolar transistor providing a pulse waveform whose frequency is proportional to the input voltage. This output requires a pull up resistor and interfaces directly with MOS, CMOS and TTL logic.

Freq/2 Out — This output is an open-collector bipolar transistor providing a square wave that is one-half the frequency of the pulse frequency output. This output requires a pull up resistor and interfaces directly with MOS, CMOS, and TTL logic.

Output Common — The emitters of both the freq/2 out and the pulse freq out are connected to this pin. An output level swing from the collector voltage to ground or to the V_{SS} supply may be obtained by connecting to the appropriate point.

R_{BIAS} — Specifications for the 9400 are based on R_{BIAS} = 100K ±10% unless otherwise noted. R_{BIAS} may be varied between the range of $82K \leq R_{BIAS} \leq 120K$.

Amplifier Out — The output stage of the operational amplifier. A negative going ramp signal is available at this pin in the V/F mode. In the F/V mode a voltage proportional to the frequency input is generated.

Zero Adjust — The non-inverting input of the operational amplifier. The low frequency set point is detemined by adjusting the voltage at this pin.

I_{IN} — The inverting input of the operational amplifier and the summing junction when connected in the V/F mode. An input current of 10μA is specified for nominal full scale but an over range current up to 50μA can be used without detrimental effect to the circuit operation.

V_{REF} — A reference voltage from either a precision source or the V_{SS} supply may be applied to this pin. Accuracy will be dependent on the voltage regulation and temperature characteristics of the circuitry.

V_{REF} OUT — The charging current for C_{REF} is derived from the internal circuitry and switched by the break-before-make switch to this pin.

V/F Design Information

Input/Output Relationships — The output frequency is related to the analog input voltage (V_{IN}) by the transfer equation:

$$\text{Frequency Out} = \frac{V_{IN}}{R_{IN}} \times \frac{1}{(V_{REF})\,(C_{REF})} = f_o$$

External Component Selection

R_{IN} — The value of this component is chosen to give a full scale input current of approximately 10μA.

$$R_{IN} \cong \frac{V_{IN}\ \text{FULL SCALE}}{10\mu A}$$

Example:

$$R_{IN} \cong \frac{10V}{10\mu A} = 1M\Omega$$

V/F Design Information (Contd.)

Note that the value is an approximation, and the exact relationship is defined by the transfer equation. In practice, the value of R_{IN} typically would be trimmed to obtain full scale frequency at V_{IN} FULL SCALE (see adjustment procedure). Metal film resistors with 1% tolerance or better are recommended for high accuracy applications because of their thermal stability and low noise generation.

C_{INT} – Exact value not critical but is related to C_{REF} by the relationship:

$$3C_{REF} \leq C_{INT} \leq 10C_{REF}$$

Improved stability and linearity is obtained when $C_{INT} \geq 4C_{REF}$. Low leakage types are recommended although mica and ceramic devices can be used in applications where their temperature limits are not exceeded. Locate as close as possible to pins 12 and 3.

C_{REF} – Exact value not critical and may be used to trim the full scale frequency (see input/output relation). Glass film or air trimmer capacitors are recommended because of their stability and low leakage. Locate as close as possible to pins 5 and 3.

V_{DD}, V_{SS} – Power supplies of ±5V are recommended. For high accuracy requirements 0.05% line and load regulation and 0.1μF disc decoupling capacitors located near the pins are recommended.

Adjustment Procedure – Figure 1 shows a circuit for trimming the zero location. Full scale may be trimmed by adjusting R_{IN}, V_{REF}, or C_{REF}. Recommended procedure is as follows for a 10KHz full scale frequency.

1. Set V_{IN} to 10mV and trim the zero adjust circuit to obtain a 10Hz output frequency.
2. Set V_{IN} to 10.000V and trim either R_{IN}, V_{REF}, or C_{REF} to obtain a 10KHz output frequency.

If adjustments are performed in this order, there should be no interaction and they should not have to be repeated.

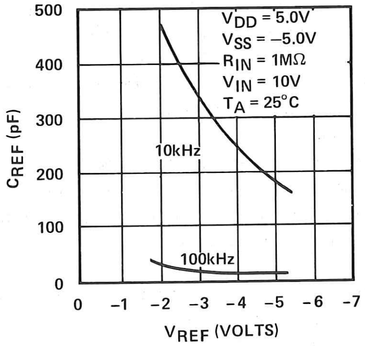
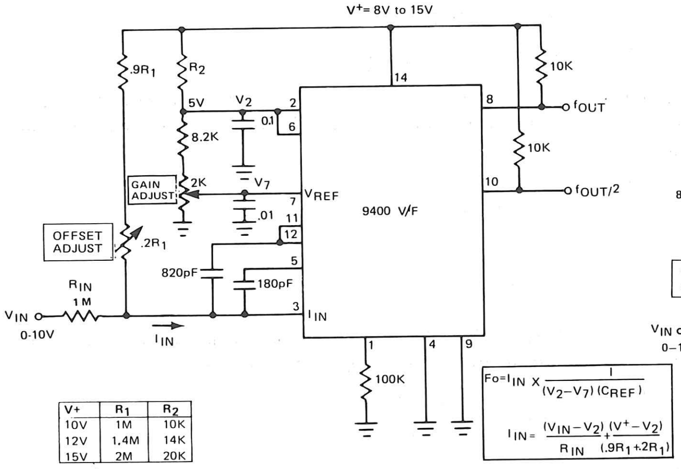


Figure 3. Recommended C_{REF} vs V_{REF}

V/F Single Supply Operation



V+	R_1	R_2
10V	1M	10K
12V	1.4M	14K
15V	2M	20K

$$F_O = I_{IN} \times \frac{1}{(V_2 - V_7)(C_{REF})}$$

$$I_{IN} = \frac{(V_{IN} - V_2)}{R_{IN}} + \frac{(V^+ - V_2)}{(.9R_1 + .2R_1)}$$

Figure 4. Fixed Voltage–Single Supply Operation

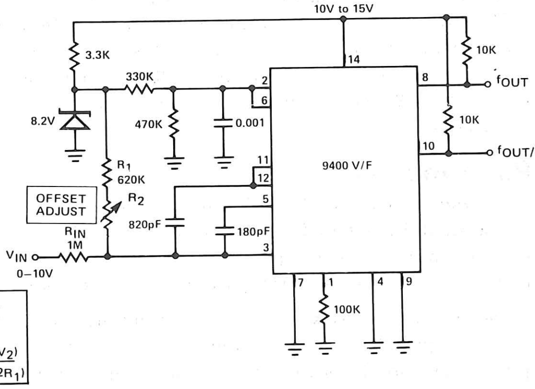


Figure 5. Variable Voltage–Single Supply Operation

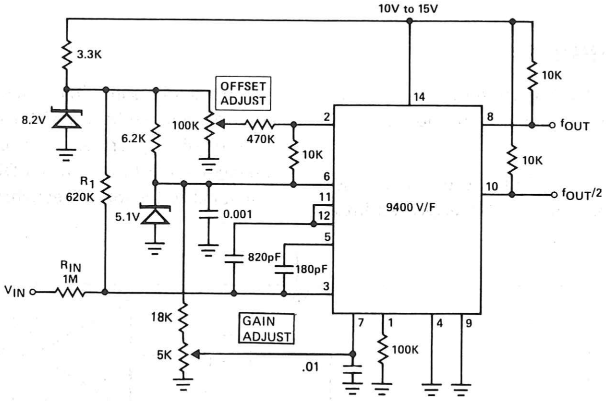


Figure 6. Single Variable Supply Voltage with Offset and Gain Adjust

Electrical Characteristics, F/V Mode

Unless otherwise specified, $V_{DD} = +5V$, $V_{SS} = -5V$, $V_{GND} = 0$, $V_{REF} = -5V$, $R_{BIAS} = 100K\Omega$, Full Scale = 10KHz. $T_A = 25°C$ unless Full Temp. Range is specified (—40° C to +85° C for N package, 0° C to 70° C for J package).

FREQUENCY-TO-VOLTAGE		9401			9400			9402				
Parameter	**Definition**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Units**	**Notes**
Accuracy Non-Linearity	Deviation from Ideal Transfer Function as a Percentage of Full Scale Voltage		0.01	**0.02**		0.02	**0.05**		0.05	**0.25**	% Full Scale	5
Input Frequency Range	Frequency Range for Specified Non-Linearity	10		100K	10		100K	10		100K	Hz	6
Frequency Inputs Positive Excursion	Voltage Required to Turn Comparator On	0.4		V_{DD}	0.4		V_{DD}	0.4		V_{DD}	V	7
Negative Excursion	Voltage Required to Turn Comparator Off	-0.4		-2V	-0.4		-2V	-0.4		-2V	V	7
Min. Positive Pulse Width	Time between Threshold Crossings		5.0			5.0			5.0		µs	7
Min. Negative Pulse Width	Time between Threshold Crossings		0.5			0.5			0.5		µs	7
Input Impedance		10			10			10			MΩ	
Analog Outputs Output Voltage	Voltage Range of Op Amp Output for Specified Non-Linearity		V_{DD}-1			V_{DD}-1			V_{DD}-1		V	8
Output Loading	Resistive Loading at Output of Op Amp	2K			2K			2K			Ω	
Supply Current I_{DD} Quiescent (N Package) (J Package)	Current Required from Positive Supply During Operation		2.0 2.0	4.0 6.0		2.0 2.0	4.0 6.0		3.0	10.0	mA mA	9
I_{SS} Quiescent (N Package) (J Package)	Current Required from Negative Supply During Operation		-1.5 -1.5	-4.0 -6.0		-1.5 -1.5	-4.0 -6.0		-3.0	-10.0	mA mA	10
V_{DD} Supply	Operating Range of Positive Supply	4.0		7.5	4.0		7.5	4.0		7.5	V	
V_{SS} Supply	Operating Range of Negative Supply	-4.0		-7.5	-4.0		-7.5	-4.0		-7.5	V	
Reference Voltage V_{REF}—V_{SS}	Range of Voltage Reference Input	-1.0			-1.0			-1.0			V	

NOTES:
1. Full temperature range.
2. $I_{IN} = 0$.
3. Full temperature range, $I_{OUT} = 10mA$.
4. $I_{OUT} = 10\mu A$.
5. 10Hz to 100KHz.
6. 5µs min. positive pulse width and 0.5µs min. negative pulse width.
7. $T_r = t_f = 20ns$.
8. $R_L \geq 2K\Omega$.
9. Full temperature range, $V_{IN} = -0.1V$.
10. $V_{IN} = -0.1V$.
11. I_{IN} connects the summing junction of an operational amplifier. Voltage sources cannot be attached directly but must be buffered by external resistors.

F/V Circuit Description

The 9400, when used as a frequency to voltage converter, generates an output voltage which is linearly proportional to the input frequency waveform.

Each zero crossing at the comparator's input causes a precise amount of charge ($q = C_{REF} \times V_{REF}$) to be dispensed into the op amp's summing junction. This charge in turn flows through the feedback resistor generating voltage pulses at the output of the op amp. A capacitor (C_{INT}) across R_{INT} averages these pulses into a DC voltage which is linearly proportional to the input frequency.

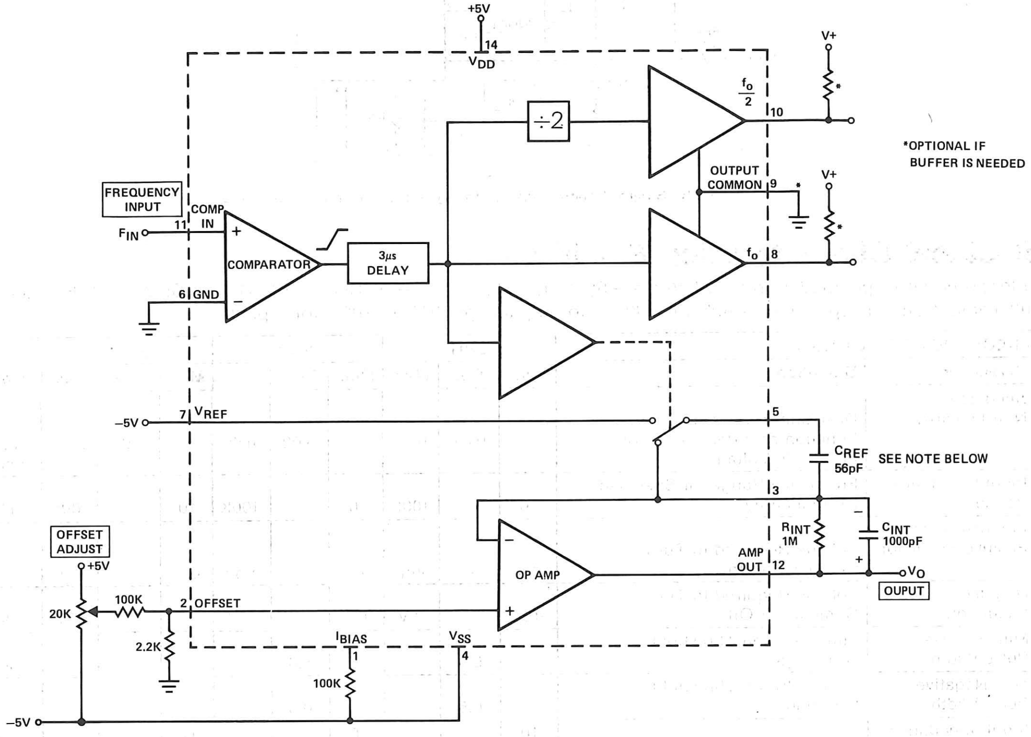


Figure 7. DC — 10KHz F/V Converter

F/V Design Information

Input/Output Relationships — The output voltage is related to the input frequency (F_{IN}) by the transfer equation:

$$V_{OUT} = \left[V_{REF}\, C_{REF}\, R_{INT}\right] F_{IN}$$

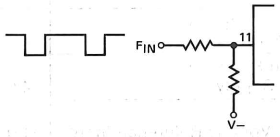
The response time to a change in F_{IN} is equal to ($R_{INT}\,C_{INT}$). The amount of ripple on V_{OUT} is inversely proportional to C_{INT} and the Input Frequency.

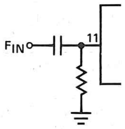
C_{INT} can be increased to lower the ripple. 1μF to 100μF are perfectly acceptable values for low frequencies.

When 9400 is used in the single supply mode, V_{REF} is defined as the voltage difference between Pin 7 and Pin 2.

Input Voltage Levels — The input signal must cross through zero in order to trip the comparator. In order to overcome the hysteresis the amplitude must be greater than ±200mV.

If only a unipolar input signal (F_{IN}) is available, it is recommended that either an offset circuit using resistor be used or that the signal be coupled in via a capacitor.





Note: C_{REF} should be increased for lower F_{IN} max. Adjust C_{REF} so that V_O is approximately 2.5 to 3.0 volts for the maximum input frequency. When F_{IN} max is less than 1 kHz, the duty cycle should be greater than 20% to insure that C_{REF} is fully charged and discharged.

F/V Design Information (Contd.)

For 100KHz maximum input R_{INT} should be decreased to 100KΩ.

Input Buffer — f_O and $f_O/2$ are not used in the F/V mode. However, these outputs may be useful for some applications, such as a buffer to feed additional circuitry. f_O will then follow the input frequency waveform; except that f_O will go high 3μs after F_{IN} goes high. $f_O/2$ will be square wave with a frequency of one half f_O.

If these outputs are not used, then Pins 8, 9 and 10 may be left floating or connected to ground.

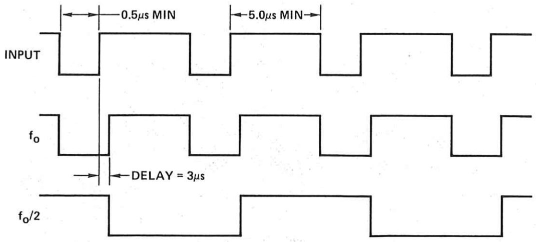
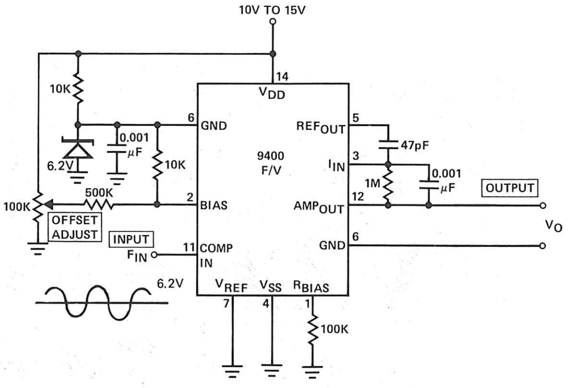


Figure 8. F/V Digital Outputs



1. The input is now referenced to 6.2 V (Pin 6). The input signal must therefore be restricted to be greater than 4 volts (Pin 6 −2V) and less than 10 to 15V (V_{DD}).

If the signal is AC coupled then a resistor (100K to 10MΩ) must be placed between the input (Pin 11) and Pin 6.

2. The output will now be referenced to Pin 6 which is at 6.2 V(V_Z). For frequency meter applications a 1mA meter with a series scaling resistor can be placed across Pins 6 and 12.

Figure 9. F/V Single Supply

The sawtooth ripple which is on the output of an F/V can be eliminated without affecting the F/V's response time by using the circuit in Figure 10. The circuit has a DC gain of +1. Any AC components such as a ripple are amplified both positively, via the lower path, and negatively, via the upper path. When both paths have the same gain, the AC ripple is cancelled. The amount of cancellation is directly proportional to gain matching. If the two paths are matched within 10%, then the ripple will be lowered by 1/10. For 1% matching, the ripple is lowered by 1/100. The 10K potentiometer is used to make the gain equal in both paths. This circuit is insensitive to both frequency changes and to signal wave shape.

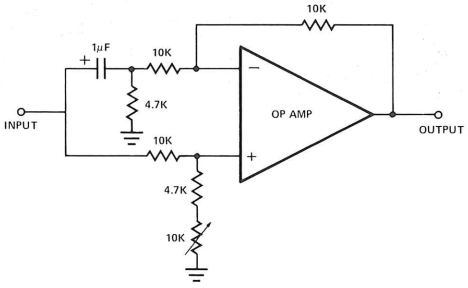
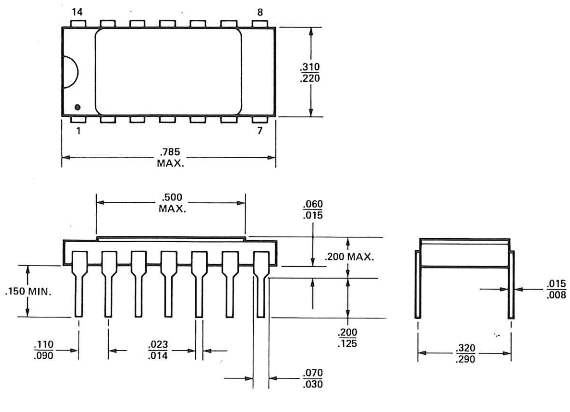
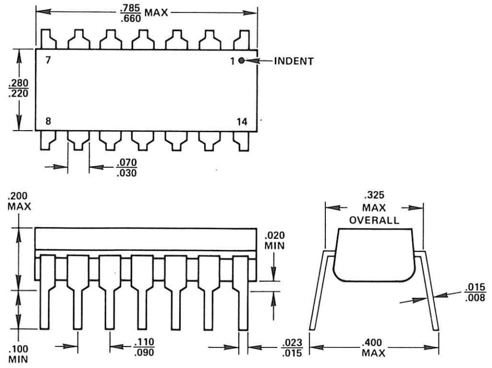


Figure 10. F/V Ripple Eliminator

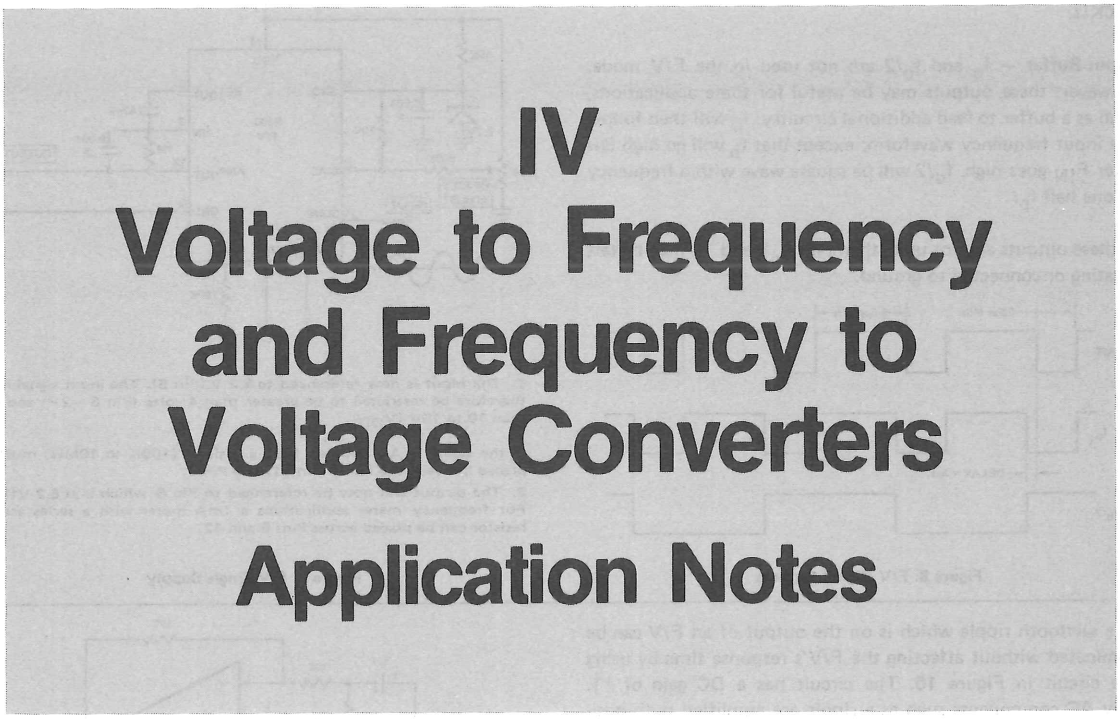
Physical Dimensions



N Package
14-Pin Ceramic DIP



J Package
14-Pin Plastic DIP



IV

Voltage to Frequency and Frequency to Voltage Converters

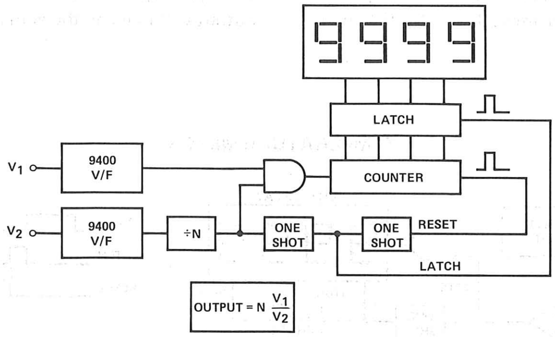
Application Notes

Applications of the 9400 Voltage to Frequency Frequency to Voltage Converter

AN-10

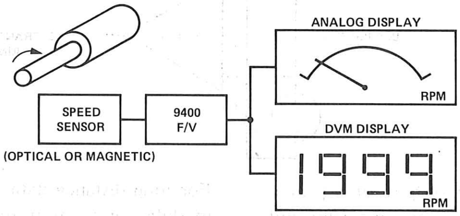
Michael O. Paiva
January 1978

RATIOMETRIC MEASUREMENT (ANALOG DIVISION)



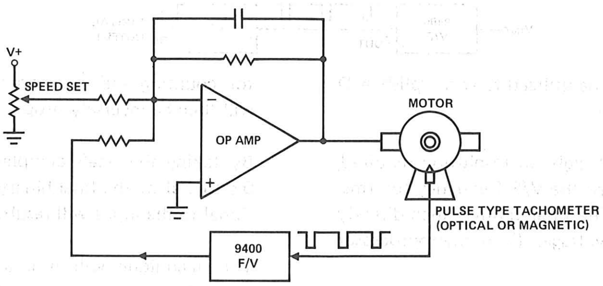
One of the most difficult circuits to build is one which will divide one analog signal by another. Two V/F converters can do such division with ease. The numerator is counted directly as a signal, while the denominator forms the time base.

RPM/SPEED INDICATOR



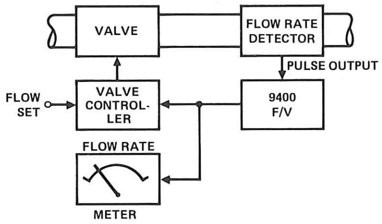
Flow rates and revolutions per second are nothing more than frequency signals since they measure the number of events per time period. Optical and magnetic sensors will convert these flows and revolutions into a digital signal which in turn can be converted to a proportional voltage by the use of an F/V converter. A simple voltmeter will then give a visual indication of the speed.

MOTOR SPEED CONTROL



The motor's speed is measured with the F/V, which converts RPM into a proportional voltage. This voltage is used in a negative feedback system to maintain the motor at the controlled setting.

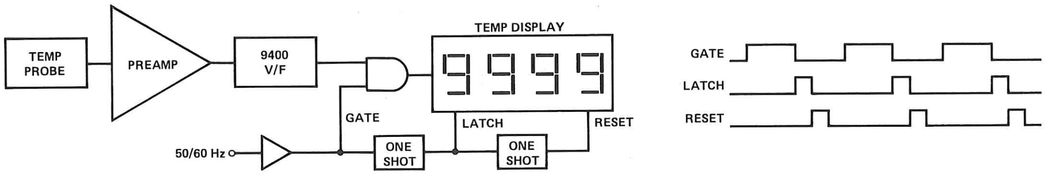
PROPORTIONAL FLOW RATE CONTROLLER

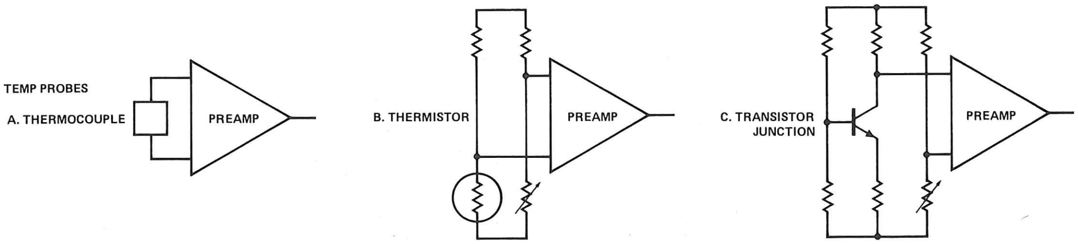


A 9400 F/V can be used to regulate the amount of liquid or gas flowing through a pipeline.

The flow rate detector generates a pulse train whose frequency is proportional to the rate of flow through it. The F/V converts this frequency to a proportional analog voltage which is used to drive the valve controller. The valve controller regulates the valve so that the flow is steady even though pipeline pressure goes up and down. A voltmeter connected to the F/V output will indicate the actual instantaneous flow rate.

TEMPERATURE METER

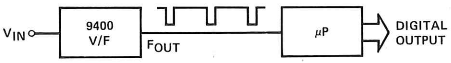




A temperature meter using the voltage output of a probe, such as one of the three shown, can be economically and straightforwardly implemented with the 9400 V/F. The V/F output is simply counted to display the temperature.

For long distance data transmission, the 9400 can be used to modulate an RF transmitter.

A/D CONVERSION WITH A MICROPROCESSOR



There are two schemes that can be utilized to accomplish A/D conversion with a microprocessor:

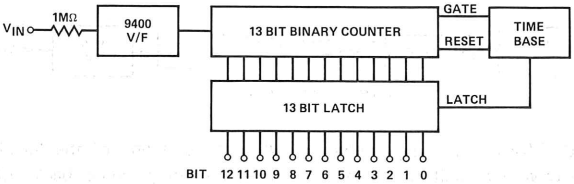
1. Depending on the number of digits of resolution required, V_{OUT} is measured by counting the V/F frequency for 1ms, 10ms, 100ms, or 1 second. The final count is then directly proportional to the input voltage. (The microprocessor provides the time base.)

2. V_{IN} is measured by determining the time between two pulses (negative edges). The F_{OUT} signal is used as a gate for counting the microprocessor's clock. The final count will then be inversely proportional to the input signal.

By taking the one's complement (changing 1's to 0's and 0's to 1's) of the final binary count a value directly proportional to the input will result.

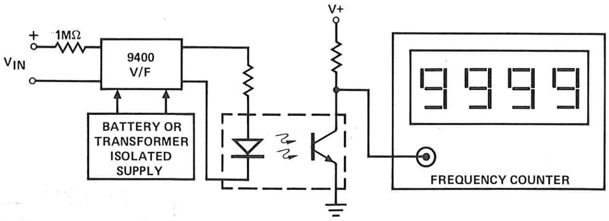
This technique will give a faster conversion time when resolution is very important, but dynamic range is limited.

13 BIT A/D CONVERTER



A 13 bit binary or 4 digit BCD A/D converter can be built by combining the 9400 V/F with a counter, latch and time base. When the V/F is set up for 10KHz full scale a 1 second time base will provide one conversion per second.

4 DIGIT VOLTMETER W/OPTO-ISOLATED INPUT

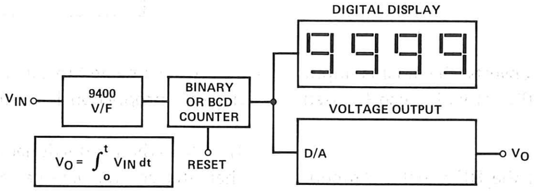


The use of a frequency counter will give a display of the V/F's frequency which is directly proportional to the input voltage.

When the V/F is running at 10KHz full scale, a 0.1 second time base will give 3 digit resolution with 10 readings per second.

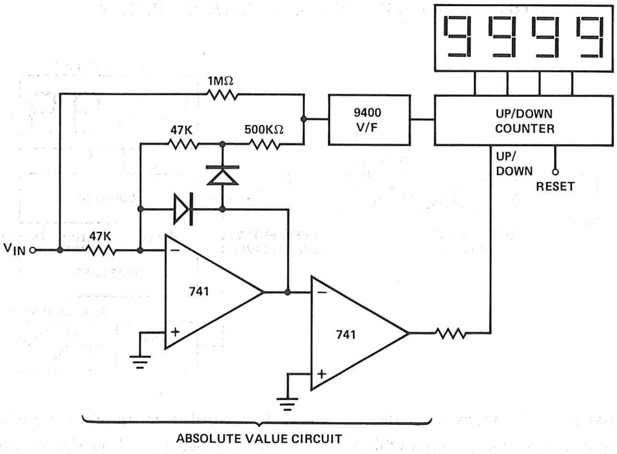
The opto isolator is used for transmitting the frequency so that there is no DC path to the frequency counter. This is especially handy in medical applications where a voltage probe should not be directly connected to a human body.

LONG TERM INTEGRATOR WITH INFINITE HOLD



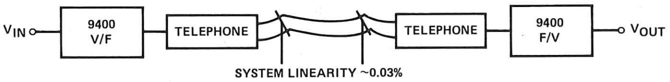
This system will integrate an input signal for minutes or days and hold its output indefinitely. The data is held in a digital counter and will stay there until the counter is reset. Typical applications involve controlling the amount of surface metal deposited in a plating system or how much charge a battery has taken on.

LONG TERM INTEGRATOR FOR BIPOLAR (+/–) SIGNALS



When the input signal is negative as well as positive there needs to be a way of generating "negative" frequencies. An absolute value circuit accomplishes this by giving the V/F a positive voltage only; and also telling the counter to count up for a positive voltage and to count down for a negative voltage.

ANALOG SIGNAL TRANSMISSION OVER TELEPHONE LINES

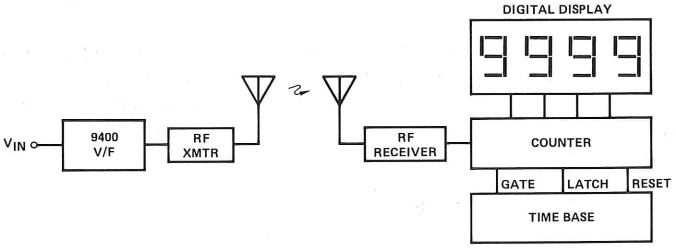


The 9400's square wave output is ideal for transmitting analog data over telephone lines. A square wave is actually preferred over a pulse waveform for data transmission since the square wave takes up less frequency spectrum than a pulse waveform.

The square wave's spectrum can be further reduced by use of low pass filters.

At the other end of the telephone line a 9400 F/V converts the frequency signal back into a voltage output which is linearly proportional to the original input voltage.

TELEMETRY

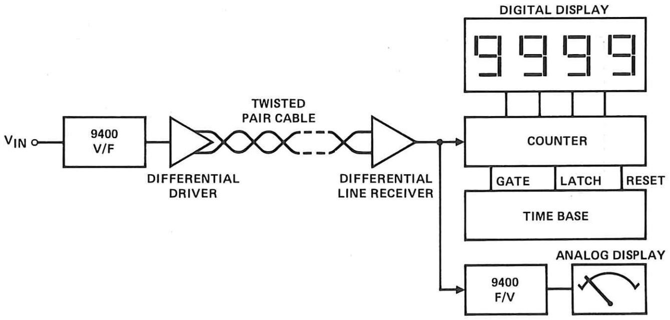


In a telemetry system the 9400 converts the analog input (V_{IN}) into frequencies (10Hz to 100KHz) which can be used to modulate an RF transmitter.

At the other end a receiver picks up the RF signal and modulates it back into the 10Hz to 100KHz spectrum. A frequency counter connected to this signal will then give a count which is linearly proportional to the original analog voltage (V_{IN}).

If a linearly proportional analog output voltage is required, then the counter can be replaced by a 9400 used in the F/V mode.

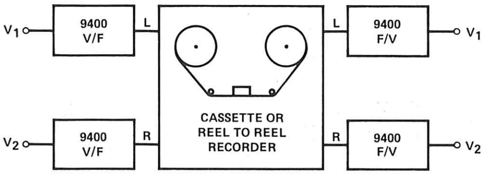
HIGH NOISE IMMUNITY DATA TRANSMISSION



When transmitting analog data over long distances it is advantageous to convert the analog signal into a digital signal which will be less susceptible to noise pick-up.

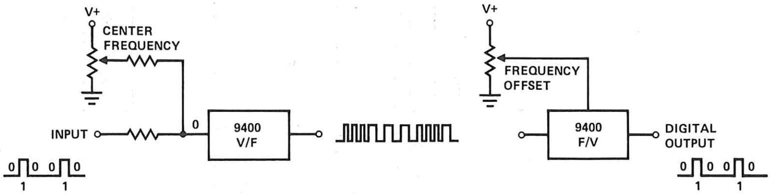
In the above system the 9400 converts the input voltage into either a pulse or square wave which is transmitted on a pair of wires by use of a line driver and receiver. At the other end the original voltage (V_{IN}) can be digitally displayed on a frequency counter or converted back to an analog voltage by use of a 9400 F/V converter.

DC RESPONSE DATA RECORDING SYSTEM



Low frequency analog data (DC to 10KHz) can be recorded anywhere, stored and then reproduced. By varying the playback speed, the frequency spectrum of the original data can be shifted up or down.

FSK GENERATION AND DECODING



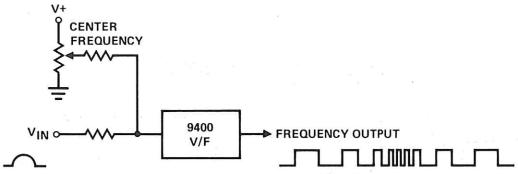
Frequency shift keying (FSK) is a simple means of transmitting digital data over a signal path (two wires, telephone lines, AM transmitters or FM transmitters).

Typically only two frequencies are transmitted. One corresponds to a logical "0" while the other corresponds to a logical "1".

A 9400 V/F will generate these two frequencies when connected as shown above. The potentiometer sets the V/F to the lower frequency. The digital input will then determine which frequency is selected. A "0" selects the lower frequency while a "1" selects the upper frequency.

The digital frequency signal is converted back into a digital format by a 9400 used in the F/V mode.

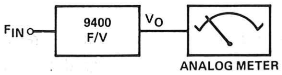
ULTRA LINEAR FREQUENCY MODULATOR



Since the 9400 is a very linear V/F converter an FM modulator is very easy to build.

The potentiometer determines the center frequency while V_{IN} will determine the amount of modulation (FM deviation) around the center frequency. V_{IN} can be negative as well as positive.

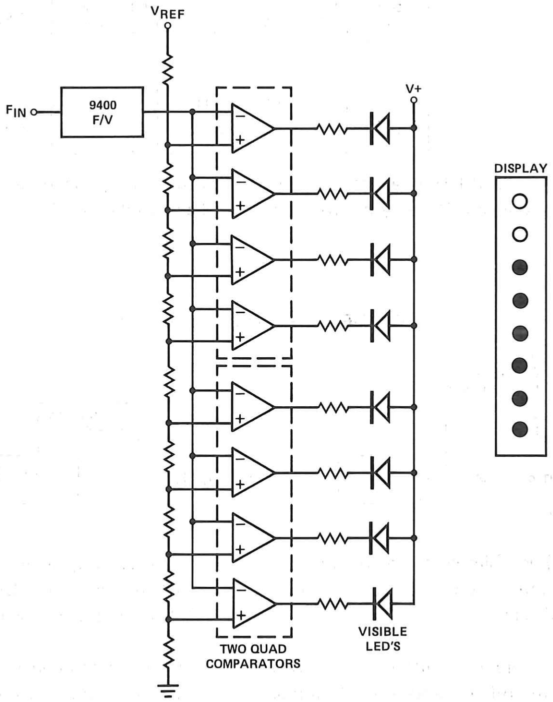
FREQUENCY METER



The 9400 will convert any frequency below 100KHz into an output voltage, which is linearly proportional to the input frequency. The equivalent frequency is then displayed on an analog meter.

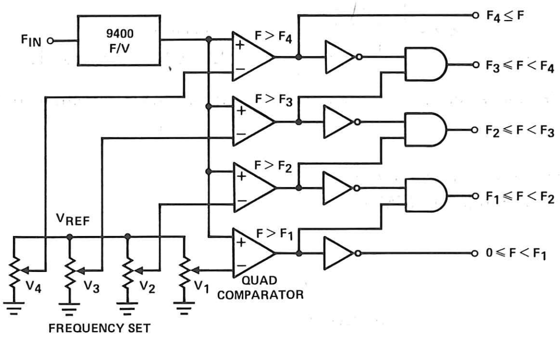
If the incoming frequency is above 100KHz a frequency divider in front of the 9400 can be used to scale the frequency down to the 100KHz region.

TACHOMETER BAR GRAPH DISPLAY



A tachometer can be constructed by using the 9400 in the F/V mode to convert the frequency information (RPM) into a linearly proportional voltage. This voltage is then compared to one of n comparators (8 in this example). When the voltage exceeds the trip point of a comparator the respective LED will light up and continue to stay lit as long as the voltage exceeds the trip point. This will give a bar graph type display with the height of the bar being proportional to RPM.

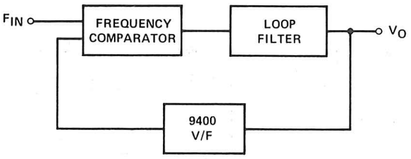
FREQUENCY/TONE DECODER



The frequency or tone to be detected is converted into a proportional analog voltage by the 9400 F/V converter. The quad comparators sense when the voltage (frequency) exceeds any of the four preset frequency limits. A logical "1" at any of the five outputs indicates that the frequency is within those limits.

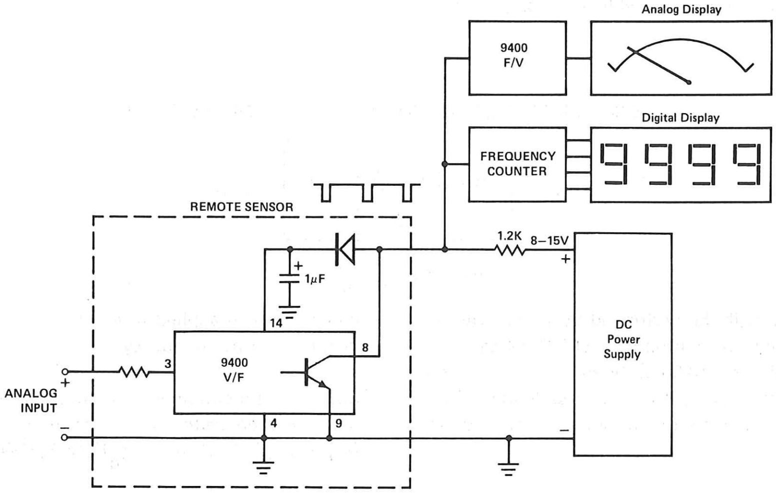
This system is useful for determining which frequency band a signal is in or for remote control where each frequency band corresponds to a different command.

FM DEMODULATION WITH A PHASE LOCKED LOOP



The high linearity of the 9400 (0.01%) is used to greatly improve the performance of a phase locked loop, resulting in very precise tracking of V_O with respect to F_{IN}.

ANALOG DATA TRANSMISSION ON DC SUPPLY LINES (TWO WIRE TRANSMITTER)



By converting an analog voltage to a linearly proportional pulse train of short duration, it is possible to transmit this data on the same wires that are used to energize the V/F converter.

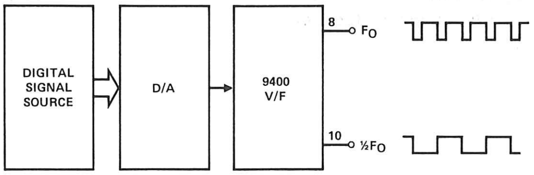
The 9400 V/F shorts out the DC supply for 3µs out of each period. At 100KHz the supply line is down 30% of the 10µs period. As the frequency is lowered the down time decreases so that at 1KHz the line is down only 0.3% of the time.

Two precautions are necessary to assure that the system does not stop functioning during the shorting period. At the power supply end a 1.2K resistor limits the current to 10mA on a 15V supply line. This prevents the 9400 from being operated beyond its output rating and at the same time it prevents the supply from being shorted out. At the V/F end a capacitor is used to keep the 9400 energized while the diode keeps the capacitor from being discharged.

Since the 9400 requires only 2mA of current, a 1µF capacitor ensures a stable voltage (the ripple is only 6mV). Since the 3µs pulses appear at the left side of the 1.2K resistor, it is easy to sense the signal here and convert the data back into a recognizable format. A frequency counter connected at this point will directly display the input voltage by counting the frequency.

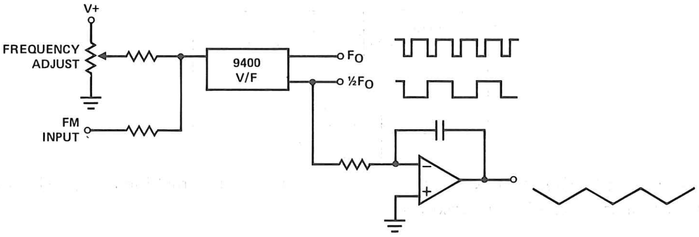
If an analog output is required, a 9400 in the F/V mode can be used to convert the frequency back into a voltage. The overall linearity is in the order of 0.03%, when both V/F and F/V are used. If only the V/F is used, then 0.01% linearity can easily be achieved.

DIGITALLY CONTROLLED FREQUENCY SOURCE



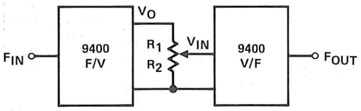
This system generates frequencies which are controlled by a microprocessor counter, register, or by thumb-wheel switches. Applications for such a system include computer controlled test equipment and numerically controlled machine tools.

WIDE FREQUENCY RANGE PULSE GENERATOR



The 9400 V/F is useful in the laboratory as a portable, battery operated low cost frequency source. The 9400 provides both pulse and square wave outputs. By adding an Op Amp integrator, a triangular waveform can also be generated. The outputs can be frequency modulated via the FM input.

FREQUENCY MULTIPLIER/DIVIDER WITH INFINITE RESOLUTION

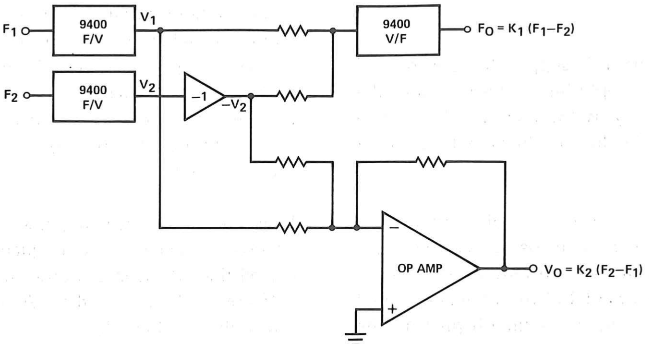


$$F_{OUT} = K_1K_2\left(\frac{R_2}{R_1+R_2}\right)F_{IN}$$

Frequency scaling can easily be performed by first converting the incoming frequency into a proportional DC voltage. This is accomplished by using the 9400 in the F/V mode. Once the frequency is in a voltage format it is easy to scale this voltage up or down by use of a single potentiometer. The resultant voltage is then applied to a 9400 V/F which generates a proportional output frequency.

Since the potentiometer is infinitely variable, the division/multiplication factor can be any number, including fractions, (K_1 is simply V_O/F_{IN} while K_2 is F_O/V_{IN}).

FREQUENCY DIFFERENCE MEASUREMENT



Frequency difference measurement is accomplished by using two 9400's in the F/V mode to convert both frequencies into two proportional analog voltages (V_1 and V_2). V_2 is inverted by a unity gain inverter. V_1 and $-V_2$ are then added by the summing Op Amp to give a voltage proportional to the frequency difference between F_2 and F_1.

Since the 9400 V/F input is actually the summing junction to an Op Amp, V_1 and $-V_2$ can be summed at the 9400 input to generate a frequency output which is proportional to the difference between F_1 and F_2.

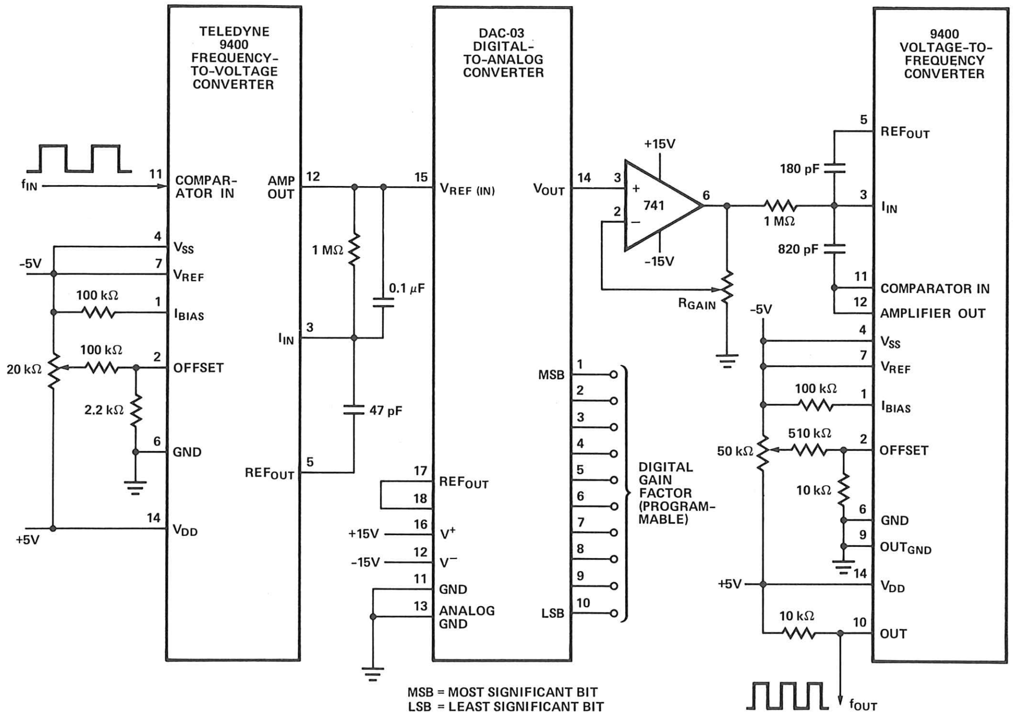
CONVERTERS SIMPLIFY DESIGN OF FREQUENCY MULTIPLIER*

By using a programmable digital-to-analog converter in combination with frequency-to-voltage and voltage-to-frequency converters, this circuit can multiply an input frequency by any number. Because it needs neither combinational logic nor a high-speed counter, it is more flexible than competing designs, uses fewer parts, and is simpler to build.

As shown in the figure, the V/F converter, a Teledyne 9400, transforms the input frequency into a corresponding voltage. An inexpensive device, the converter requires only a few external components for setting its upper operating frequency as high as 100 kilohertz.

Next the signal is applied to the reference port of the DAC-03 d-a converter, where it is amplified by the frequency-multiplying factor programmed into the converter by thumbwheel switches or a microprocessor. The d-a converter's output is the product of the analog input voltage and the digital gain factor.

R_3 sets the gain of the 741 op amp to any value, providing trim adjustment or a convenient way to scale the d-a converter's output to a much higher or lower voltage for the final stage, a 9400 converter that operates in the voltage-to-frequency mode. The 741 and R_3 can also be used to set circuit gain to non-integer values. The V/F device then converts the input voltage into a proportionally higher or lower frequency.



Circuit uses frequency-to-voltage-to-frequency conversion, with intermediate stage of gain between conversions, for multiplying input frequency by any number. Digital-to-analog converter is programmed digitally, by thumbwheel switches or microprocessor, for coarse selection of frequency-multiplying factor; 741 provides fine gain, enables choice of non-integer multiplication values.

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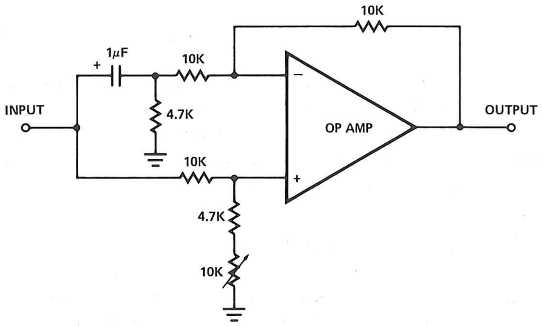
F/V RIPPLE ELIMINATOR

Output ripple can be eliminated from the 9400 F/V converter by a simple process. The circuit diagram on the right shows a new method that eliminates ripple when connected to pin 12 of the 940 used in the F/V mode.

The sawtooth ripple which is on the output of an F/V can be eliminated without affecting the F/V's response time by using the circuit in the above figure. The circuit has a DC gain of ±1. Any AC components such as a ripple are amplified both positively, via the lower path, and negatively, via the upper path. When both paths have the same gain, the AC ripple is cancelled. The amount of cancellation is directly proportional to gain matching. If the two paths are matched within 10%, then the ripple will be lowered by 1/10. For 1% matching, the ripple is lowered by 1/100. The 10K potentiometer is used to make the gain equal in both paths. This circuit is insensitive to both frequency changes and to signal wave shape.



F/V Ripple Eliminator for 9400 F/V

V

Monolithic Voltage References

Monolithic Voltage Reference

9491

1.22 Volts

Features

- Guaranteed temperature coefficient: 50 or 100 ppm/°C
- Low bias current: 50μA
- Low breakdown voltage: 1.22V
- Low dynamic impedance 2Ω max.
- TO-18 or TO-92 package
- Low Cost

Applications

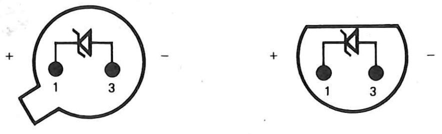
- Reference for A/D and D/A converters
- Threshold detectors
- Voltage Regulators
- VOM and VTVM's
- Amplifier biasing
- Battery operated equipment

General Description

The 9491 is a 1.22V temperature compensated voltage reference. It uses the band-gap principal to achieve extremely tight regulation over a wide range of operating currents. The use of thin film resistors assures long term stability and low noise.

Connection Diagram

Bottom Views



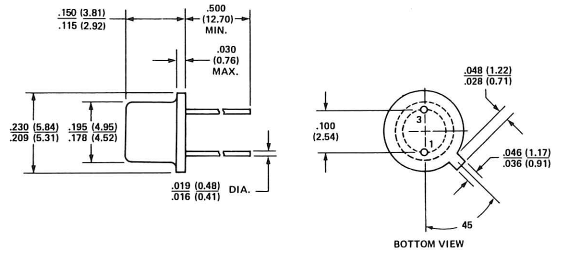
TO-18 **TO-92**

Ordering Information

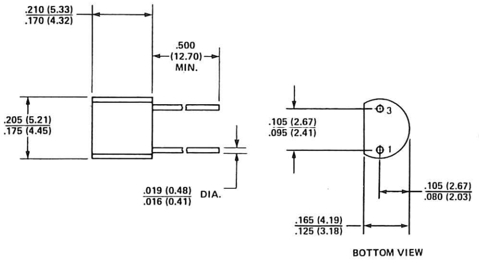
	Temperature Range	
Temp. Coeff.	−55°C to +125°C (TO-18)	0°C to 70°C (TO-92)
50 ppm/°C	9491AM	9491AJ
100 ppm/°C	9491BM	9491BJ

Packaging Information

TO-18
(2 PIN)



TO-92
(2 PIN)



All dimensions in inches (millimeters)

Absolute Maximum Ratings

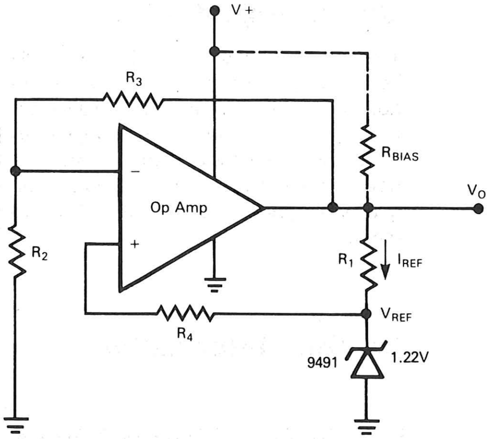
	TO-18	TO-92
Storage Temperature	−65°C to +200°C	−55°C to +150°C
Operating Temperature	−55°C to +125°C	0°C to +70°C
Forward Current, Max.	5mA	5mA
Reverse Current, Max.	5mA	5mA
Power Dissipation	Limited by max forward/reverse current	
Lead Temperature (Soldering, 10 seconds)	300°C	260°C

Electrical Characteristics (T$_A$ = 25°C unless otherwise noted)

Parameters		Min	Typ	Max	Units	Conditions
Reverse Breakdown Voltage	B_{VR}	1.20	1.22	1.25	V	$I_R = 500\mu A$
Reverse Breakdown Voltage Change	ΔB_{VR}	—	15	20	mV	$50\mu A < I_R < 5mA$
Reverse Dynamic Impedance	Z_R	—	1 1	2 2	Ω Ω	$I_R = 50\mu A$ $I_R = 500\mu A$
Temp. Coefficient 9491B	$\frac{\Delta B_{VR}}{\Delta T}$		.003	0.01	%/°C	$50\mu A < I_R < 5mA$
9491A			.003	0.005		
Reverse Current	I_R	0.05	—	5.0	mA	

Applications/Design Circuits

Adjustable Voltage Reference



$$V_O = V_{REF}\left(\frac{R_2 + R_3}{R_2}\right)$$

$$I_{REF} = \frac{V_O - V_{REF}}{R_1}$$

$$R_4 = \frac{R_2 \cdot R_3}{R_2 + R_3}$$

Monolithic Voltage Reference

9495

5 Volts

Features

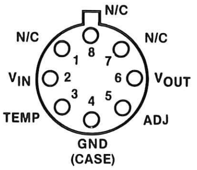
- Excellent Temperature Stability: 3ppm/°C
- Choice of Tolerance: 0.3 and 1%
- Adjustable Output
- Input Voltage Range: 7V to 40V
- Low Noise: 15 μVpp max.
- 10mA Output Current
- Short Circuit Proof
- Low Power: 1.4mA
- Temperature Output
- Mil-STD-883 Screening Available
- Replaces REF-02

Applications

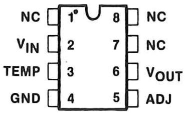
- A/D Reference
- D/A Reference
- Current Source
- Transducer Reference
- Calibration Standard
- Thermometer

Connection Diagram

TOP VIEW

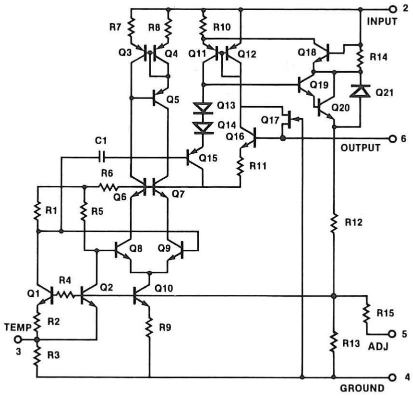


TO-99



8 PIN PLASTIC MINI DIP

Schematic Diagram



General Description

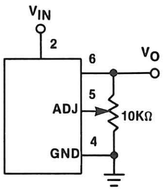
The 9495, Precision Voltage Reference, uses the band gap principle to generate an extremely stable 5 volt reference. Included in the 9495 are a band gap reference, an output amplifier and a voltage which varies linearly with temperature. The reference is ideal because of its low cost, low output noise and low power requirement. The 9495 is exceptionally stable over wide variations in temperature, line voltage and load current. The reference operates on a single supply with voltages of 7 volts to 40 volts.

The 9495 is available with initial accuracies of ±0.3% or ±1%. An external potentiometer can be used to vary the output voltage ±6% with little effect on the temperature coefficient. The potentiometer can also be used to adjust the voltage for binary applications such as 5.12 volts.

Pin 3 of the 9495 has available a voltage which varies linearly with temperature. The typical change is 2.1 mv/°C, or 460mV to 840mV over the −55°C to +125°C temperature range. By using a buffer amplifier, the output voltage can be scaled to the desired resolution and range.

Output Adjustment

The output voltage of the 9495 can easily be adjusted by connecting a potentiometer to pin 5 as shown in the adjacent figure. Changing the output voltage does affect the overall temperature coefficient, however, this effect is small being typically only 0.7 ppm/°C per 100mV of adjustment.



Ordering Information

Initial Accuracy	Max. Temp. Coeff	Temperature Range	Maximum Voltage	Part Number To-99 Package	 8 Pin Mini-Dip
0.3%	8.5ppm	0 - 70°C	40V	9495EE	—
1.0%	65ppm	0 - 70°C	30V	9495CE	9495CJ
0.3%	8.5ppm	−55° to +125°C	40V	9495AE	—

	9495 AE	
Initial Accuracy Max. Temp. Coeff. Temperature Range	0.3% 8.5ppm/°C $-55°C$ to $+125°C$	

These specifications apply for V_{IN} = +15V, $T_A = 25°C$, unless otherwise noted.

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Output Voltage	V_O	$I_L = 0mA$	4.985	5.000	5.015	V
Output Adjustment Range	ΔV_{trim}	$R_p = 10k\Omega$	±3.0	±6.0	—	%
Output Voltage Noise	$e_{np\text{-}p}$	0.1Hz to 10Hz	—	10	15	μVp-p
Input Voltage Range	V_{IN}		7	—	40	V
Line Regulation (Note 1)		$V_{IN} = 8$ to 33V	—	0.006	0.010	%/V
Load Regulation (Note 1)		$I_L = 0$ to 10mA	—	0.005	0.010	%/mA
Turn-on-Settling Time	t_{on}	To 0.1% of final value	—	5.0	—	μsec
Quiescent Supply Current	I_{SY}	No Load	—	1.0	1.4	mA
Load Current	I_L		10	21	—	mA
Sink Current	I_S		−0.3	−0.5	—	mA
Short Circuit Current	I_{SC}	$V_O = 0$	—	30	—	mA
Temp Voltage Output	V_T	(Note 2)	—	630	—	mV

The following specifications apply for V_{IN} = +15V, $-55°C \le T_A \le +125°C$ and I_L = 0mA, unless otherwise noted

Output Voltage Change with Temperature (Note 3)	ΔV_{OT}	$0° \le T_A \le +125°C$	—	0.02	0.06	%
		$-55° \le T_A \le +125°C$		0.06	0.15	%
Output Voltage Temperature Coefficient	TCV_O	(Note 4)	—	3	8.5	ppm/°C
Change in V_O Temperature Coefficient with Output Adjustment		$R_p = 10K\Omega$	—	0.7	—	ppm/%
Line Regulation (Note 1) $V_{IN} = 8$ to 33V		$0° \le T_A \le +70°C$	—	0.007	0.012	%/V
		$-55° \le T_A \le +125°C$	—	0.009	0.015	%/V
Load Regulation (Note 1) ($I_L = 0$ to 8mA)		$0° \le T_A \le +70°C$	—	0.006	0.010	%/mA
		$-55° \le T_A \le +125°C$	—	0.007	0.012	%/mA
Temp Voltage Output Temperature Coefficient	TCV_T	(Note 2)	—	2.1	—	mV/°C

NOTE 1 Line and Load Regulation specifications include the effects of self heating.

NOTE 2 Limit current in or out of pin 3 to 50nA and capacitance on pin 3 of 30pF.

NOTE 3 ΔV_{OT} is defined as the absolute difference between the maximum output voltage and minimum output voltage over the specified temperature range expressed as a percentage of 5V:

$$\Delta V_{OT} = \frac{V_{MAX}\text{-}V_{MIN}}{5V} \times 100$$

NOTE 4 TCV_O is defined as ΔV_{OT} divided by the temperature range, i.e., $TCV_O\ (-55° \text{ to } +125°C) = \frac{\Delta V_{OT}\ -55° \text{ to } +125°C}{180°C}$

Absolute Maximum Ratings

Input Voltage	40V
Power Dissipation	500mW
Derating: To-99, above 80°C ambient	7.1mW/°C
Operating Temperature:	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

Definitions

Line Regulation
The ratio of the change in output voltage to the change in line voltage producing it.

Load Regulation
The ratio of the change in output voltage to the change in load current producing it.

Quiescent Current (I_{SY})
The current required from the supply to operate the device with no load.

Output Voltage Noise ($e_{np\text{-}p}$)
The peak to peak output noise voltage in a specified frequency band

Output Turn-On Settling Time (t_{on})
The time required for the output voltage to reach its final value within a specified error band after application of V_{IN}.

	9495 CE 9495 CJ	
Initial Accuracy Max. Temp. Coeff. Temperature Range	1.0% 65ppmC° 0°C to 70°C	

These specifications apply for V_{IN} = +15V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Output Voltage	V_O	$I_L = 0mA$	4.950	5.000	5.050	V
Output Adjustment Range	ΔV_{trim}	$R_p = 10k\Omega$	±2.7	±6.0	—	%
Output Voltage Noise	$e_{np\text{-}p}$	0.1Hz to 10Hz	—	12	18	μVp-p
Input Voltage Range	V_{IN}		7	—	30	V
Line Regulation (Note 1)		$V_{IN} = 8$ to 30V	—	0.009	0.015	%/V
Load Regulation (Note 1)		$I_L = 0$ to 8mA	—	0.006	0.015	%/mA
Load Regulation (Note 1)		$I_L = 0$ to 4mA	—	—	—	%/mA
Turn-on-Settling Time	t_{on}	To ±0.1% of final value	—	5.0	—	μsec
Quiescent Supply Current	I_{SY}	No Load	—	1.0	1.6	mA
Load Current	I_L		8	21	—	mA
Sink Current	I_S		−0.2	−0.5	—	mA
Short Circuit Current	I_{SC}	$V_O = 0$	—	30	—	mA
Temp Voltage Output	V_T	(Note 2)	—	630	—	mV

The following specifications apply for V_{IN} = +15V, 0°C ≤ T_A ≤ +70°C and I_L = 0mA, unless otherwise noted.

Output Voltage Change with Temperature	ΔV_{OT}	(Note 3)	—	0.14	0.45	%
Output Voltage Temperature Coefficient	TCV_O	(Note 4)	—	20	65	ppm/°C
Change in V_O Temperature Coefficient with Output Adjustment		$R_p = 10K\Omega$	—	0.7	—	ppm/%
Line Regulation (Note 1)		$V_{IN} = 8$ to 30V	—	0.011	0.018	%/V
Load Regulation (Note 1)		$I_L = 0$ to 5mA	—	0.008	0.018	%/mA
Temp Voltage Output Temperature Coefficient	TCV_T	(Note 2)	—	2.1	—	mV/°C

NOTE 1 Line and Load Regulation specifications include the effects of self heating.

NOTE 2 Limit current in or out of pin 3 to 50nA and capacitance on pin 3 to 30pF.

NOTE 3 ΔV_{OT} is defined as the absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range expressed as a percentage of 5V:

$$\Delta V_{OT} = \frac{V_{MAX} - V_{MIN}}{5V} \times 100$$

NOTE 4 TCV_O is defined as ΔV_{OT} divided by the temperature range, i.e., $TCV_O = \frac{\Delta V_{OT}}{70°C}$

Absolute Maximum Ratings

Input Voltage	30V
Power Dissipation	500mW
Derating: To-99, above 80°C ambient Mini Dip, above 30°C ambient	7.1mW/°C 5.6mW/°C
Operating Temperature:	0°C to 70°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

	9495 EE
Initial Accuracy	0.3%
Max. Temp. Coeff.	8.5ppm/°C
Temperature Range	0°C to +70°C

These specifications apply for V_{IN} = +15V, T_A=25°C, unless otherwise noted.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Output Voltage	V_O	I_L=0mA	4.985	5.000	5.015	V
Output Adjustment Range	ΔV_{trim}	R_p=10kΩ	±3.0	±6.0	—	%
Output Voltage Noise	$e_{np\text{-}p}$	0.1Hz to 10Hz	—	10	15	μVp-p
Input Voltage Range	V_{IN}		7	—	40	V
Line Regulation (Note 1)		V_{IN}=8 to 33V	—	0.006	0.010	%/V
Load Regulation (Note 1)		I_L=0 to 10mA	—	0.005	0.010	%/mA
Turn-on-Settling Time	t_{on}	To ±0.1% of final value	—	5.0	—	μsec
Quiescent Supply Current	I_{SY}	No Load	—	1.0	1.4	mA
Load Current	I_L		10	21	—	mA
Sink Current	I_S		−0.3	−0.5	—	mA
Short Circuit Current	I_{SC}	V_O=0	—	30	—	mA
Temp Voltage Output	V_T	(Note 2)	—	630	—	mV

The following specifications apply for V_{IN} = +15V, 0°C≤T_A≤+70°C and I_L = 0mA, unless otherwise noted.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Output Voltage Change with Temperature	ΔV_{OT}	(Note 3)	—	0.02	0.06	%
Output Voltage Temperature Coefficient	TCV_O	(Note 4)	—	3	8.5	ppm/°C
Change in V_O Temperature Coefficient with Output Adjustment		R_p=10KΩ	—	0.7	—	ppm/%
Line Regulation (Note 1)		V_{IN}=8 to 33V	—	0.007	0.012	%/V
Load Regulation (Note 1)		I_L=0 to 8mA	—	0.006	0.010	%/mA
Temp Voltage Output Temperature Coefficient	TCV_T	(Note 2)	—	2.1	—	mV/°C

NOTE 1 Line and Load Regulation specifications include the effects of self heating.
NOTE 2 Limit current in or out of pin 3 to 50nA and capacitance on pin 3 to 30pF.
NOTE 3 ΔV_{OT} is defined as the absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range expressed as a percentage of 5V:

$$\Delta V_{OT} = \frac{V_{MAX}-V_{MIN}}{5V} \times 100$$

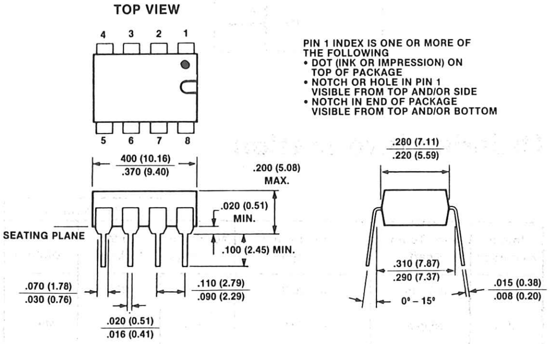
NOTE 4 TCV_O is defined as ΔV_{OT} divided by the temperature range, i.e., $TCV_O = \frac{\Delta V_{OT}}{70°C}$

Absolute Maximum Ratings

Input Voltage	40V
Power Dissipation	500mW
Derating: To-99, above 80°C ambient Mini Dip, above 30°C ambient	7.1mW/°C 5.6mW/°C
Operating Temperature:	0°C to 70°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

Packaging Information

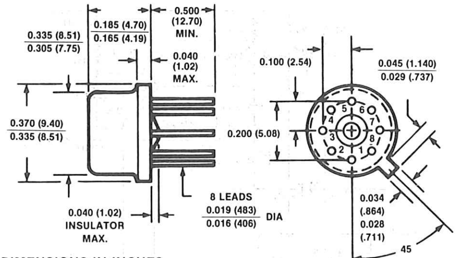
8-PIN PLASTIC MINI-DIP (SUFFIX J)



PIN 1 INDEX IS ONE OR MORE OF THE FOLLOWING
- DOT (INK OR IMPRESSION) ON TOP OF PACKAGE
- NOTCH OR HOLE IN PIN 1 VISIBLE FROM TOP AND/OR SIDE
- NOTCH IN END OF PACKAGE VISIBLE FROM TOP AND/OR BOTTOM

ALL DIMENSIONS IN INCHES.
(ALL DIMENSIONS IN MILLIMETERS)

TO-99 (SUFFIX E)



ALL DIMENSIONS IN INCHES.
(ALL DIMENSIONS IN MILLIMETERS)

BOTTOM VIEW

Monolithic Voltage Reference

9496

10 Volts

Features

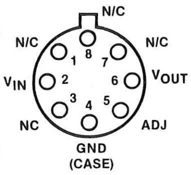
- Excellent Temperature Stability: 3ppm/°C
- Choice of Tolerance: 0.3 and 1%
- Adjustable Output
- Input Voltage Range: 12V to 40V
- Low Noise : 30 μVpp max.
- 10mA Output Current
- Short Circuit Proof
- Low Power : 1.4mA
- Mil-STD-883 Screening Available
- Replaces REF-01

Applications

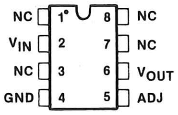
- A/D Reference
- D/A Reference
- Current Source
- Transducer Reference
- Calibration Standard

Connection Diagram

TOP VIEW

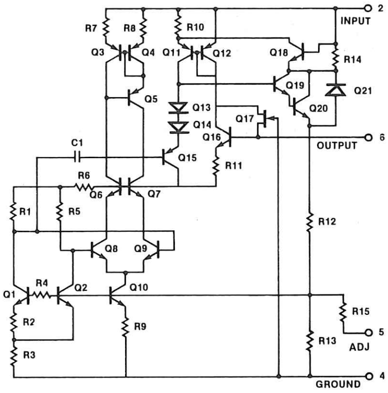


TO-99



8 PIN PLASTIC MINI DIP

Schematic Diagram



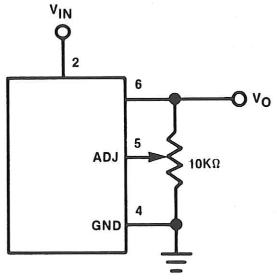
General Description

The 9496, Precision Voltage Reference, uses the band gap principle to generate an extremely stable 10 volt reference. Included in the 9496 are a band gap reference, and an output amplifier, which delivers 10mA of output current. The reference is ideal because of its low cost, low output noise and low power requirement. The 9496 is exceptionally stable over wide variations in temperature, line voltage and load current. The reference operates on a single supply with voltages of 12 volts to 40 volts.

The 9496 is available with initial accuracies of ± 0.3%, and ±1%. An external potentiometer can be used to vary the output voltage ±3% with little effect on the temperature coefficient. The potentiometer can also be used to adjust the voltage for binary applications such as 10.24 volts.

Output Adjustment

The output voltage of the 9496 can easily be adjusted by connecting a potentiometer to pin 5 as shown in the figure below. Changing the output voltage does affect the overall temperature coefficient, however, this effect is small being typically only 0.7 ppm/°C per 100mV of adjustment.



Ordering Information

				Part Number	
Initial Accuracy	Max. Temp Coeff	Temperature Range	Maximum Voltage	To-99 Package	8 Pin Mini-Dip
0.3%	8.5ppm	0 - 70°C	40V	9496EE	–
1.0%	65ppm	0 - 70°C	30V	9496CE	9496CJ
0.3%	8.5ppm	−55° to +125°C	40V	9496AE	–

	9496 AE	
Initial Accuracy **Max. Temp. Coeff.** **Temperature Range**	0.3% 8.5ppm/°C −55°C to +125°C	

These specifications apply for V_{IN} = +15V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Output Voltage	V_O	$I_L = 0mA$	9.97	10.00	10.03	V
Output Adjustment Range	ΔV_{trim}	$R_p = 10k\Omega$	±3.0	±3.3	—	%
Output Voltage Noise	$e_{np\text{-}p}$	0.1Hz to 10Hz	—	20	30	μVp-p
Input Voltage Range	V_{IN}		12	—	40	V
Line Regulation (Note 1)		V_{IN} = 13 to 33V	—	0.006	0.010	%/V
Load Regulation (Note 1)		I_L = 0 to 10mA	—	0.005	0.008	%/mA
Turn-on-Settling Time	t_{on}	To ±0.1% of final value	—	5.0	—	μsec
Quiescent Supply Current	I_{SY}	No Load	—	1.0	1.4	mA
Load Current	I_L		10	21	—	mA
Sink Current	I_S		−0.3	−0.5	—	mA
Short Circuit Current	I_{SC}	$V_O = 0$	—	30	—	mA

The following specifications apply for V_{IN} = +15V, −55°C ≤ T_A ≤ +125°C and I_L = 0mA, unless otherwise noted.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Output Voltage Change with Temperature (Note 3)	ΔV_{OT}	$0° \le T_A \le +70°C$	—	0.02	0.06	%
		$-55 \le T_A \le +125°C$	—	0.06	0.15	%
Output Voltage Temperature Coefficient	TCV_O	(Note 2)	—	3	8.5	ppm/°C
Change in V_O Temperature Coefficient with Output Adjustment		$R_p = 10K\Omega$	—	0.7	—	ppm/%
Line Regulation (V_{IN} = 13 to 33V) (Note 1)		$0° \le T_A \le +70°C$	—	0.007	0.012	%/V
		$-55° \le T_A \le +125°C$	—	0.009	0.015	%/V
Load Regulation (I_L = 0 to 8mA) (Note 1)		$0° \le T_A \le +70°C$	—	0.006	0.010	%/mA
		$-55° \le T_A \le +125°C$	—	0.007	0.012	%/mA

NOTE 1 Line and Load Regulation specifications include the effects of self heating.

NOTE 2 TCV_O is defined as ΔV_{OT} divided by the temperature range, i.e., $TCV_O(0° \text{ to } +70\ C) = \dfrac{\Delta V_{OT}\ 0° \text{ to } +70\ C}{70°C}$ and $TCV_O(-55°C \text{ to } +125°C) = \dfrac{\Delta V_{OT}\ -55°C \text{ to } +125°C}{180°C}$

NOTE 3 ΔV_{OT} is defined as the absolute difference between the maximum output voltage and minimum output voltage over the specified temperature range expressed as a percentage of 10V:

$$\Delta V_{OT} = \frac{V_{MAX} - V_{MIN}}{10V} \times 100$$

Absolute Maximum Ratings

Input Voltage	40V
Power Dissipation	500mW
Derating: To-99, above 80°C ambient	7.1mW/°C
Operating Temperature	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

Definitions

Line Regulation
The ratio of the change in output voltage to the change in line voltage producing it.

Load Regulation
The ratio of the change in output voltage to the change in load current producing it.

Quiescent Current (I_{SY})
The current required from the supply to operate the device with no load.

Output Voltage Noise ($e_{np\text{-}p}$)
The peak to peak output noise voltage in a specified frequency band

Output Turn-On Settling Time (t_{on})
The time required for the output voltage to reach its final value within a specified error band after application of V_{IN}.

	9496 CE 9496 CJ	
Initial Accuracy	**1.0%**	
Max. Temp. Coeff.	**65ppm/°C**	
Temperature Range	**0°C to 70°C**	

These specifications apply for V_{IN} = +15V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Output Voltage	V_O	$I_L = 0mA$	9.90	10.00	10.10	V
Output Adjustment Range	ΔV_{trim}	$R_p = 10k\Omega$	±2.7	±3.3	—	%
Output Voltage Noise	$e_{np\text{-}p}$	0.1Hz to 10Hz	—	25	35	µVp-p
Input Voltage Range	V_{IN}		12	—	30	V
Line Regulation (Note 1)		V_{IN} = 13 to 30V	—	0.009	0.015	%/V
Load Regulation (Note 1)		I_L = 0 to 8mA	—	0.006	0.015	%/mA
Load Regulation (Note 1)		I_L = 0 to 4mA	—	0.006	0.015	%/mA
Turn-on-Settling Time	t_{on}	To ±0.1% of final value	—	5.0	—	µsec
Quiescent Supply Current	I_{SY}	No Load	—	1.0	1.6	mA
Load Current	I_L		8	21	—	mA
Sink Current	I_S		−0.2	−0.5	—	mA
Short Circuit Current	I_{SC}	$V_O = 0$	—	30	—	mA

The following specifications apply for V_{IN} = +15V, 0°C ≤ T_A ≤ +70°C, unless otherwise noted.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Output Voltage Change with Temperature	ΔV_{OT}	(Note 3)	—	0.14	0.45	%
Output Voltage Temperature Coefficient	TCV_O	(Note 2)	—	20	65	ppm/°C
Change in V_O Temperature Coefficient with Output Adjustment		$R_p = 10K\Omega$	—	0.7	—	ppm/%
Line Regulation (Note 1)		V_{IN} = 13 to 30V	—	0.011	0.018	%/V
Load Regulation (Note 1)		I_L = 0 to 5mA	—	0.008	0.018	%/mA

NOTE 1 Line and Load Regulation specifications include the effects of self heating.

NOTE 2 TCV_O is defined as ΔV_{OT} divided by the temperature range, i.e., $TCV_O = \frac{\Delta V_{OT}}{70°C}$

NOTE 3 ΔV_{OT} is defined as the absolute difference between the maximum output voltage and minimum output voltage over the specified temperature range expressed as a percentage of 10V:

$$\Delta V_{OT} = \frac{V_{MAX} - V_{MIN}}{10V} \times 100$$

Absolute Maximum Ratings

Input Voltage	30V
Power Dissipation	500mW
Derating: To-99, above 80°C ambient Mini Dip, above 30°C ambient	7.1mW/°C 5.6mW/°C
Operating Temperature	0°C to 70°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

	9496 EE	
Initial Accuracy Max. Temp. Coeff. Temperature Range	0.3% 8.5ppm/°C 0°C to +70°C	

These specifications apply for V_{IN} = +15V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Output Voltage	V_O	$I_L = 0mA$	9.97	10.00	10.03	V
Output Adjustment Range	ΔV_{trim}	$R_p = 10k\Omega$	±3.0	±3.3	–	%
Output Voltage Noise	$e_{np\text{-}p}$	0.1Hz to 10Hz	–	20	30	μVp-p
Input Voltage Range	V_{IN}		12	–	40	V
Line Regulation (Note 1)		$V_{IN} = 13$ to 33V	–	0.006	0.010	%/V
Load Regulation (Note 1)		$I_L = 0$ to 10mA	–	0.005	0.008	%/mA
Turn-on-Settling Time	t_{on}	To ±0.1% of final value	–	5.0	–	μsec
Quiescent Supply Current	I_{SY}	No Load	–	1.0	1.4	mA
Load Current	I_L		10	21	–	mA
Sink Current	I_S		−0.3	−0.5	–	mA
Short Circuit Current	I_{SC}	$V_O = 0$	–	30	–	mA

The following specifications apply for V_{IN} = +15V, 0°C ≤ T_A ≤ +70°C and I_L = 0mA, unless otherwise noted.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Output Voltage Change with Temperature	ΔV_{OT}	(Note 3)	–	0.02	0.06	%
Output Voltage Temperature Coefficient	TCV_O	(Note 2)	–	3	8.5	ppm/°C
Change in V_O Temperature Coefficient with Output Adjustment		$R_p = 10K\Omega$	–	0.7	–	ppm/%
Line Regulation (Note 1)		V_{IN} = 13 to 33V	–	0.007	0.012	%/V
Load Regulation (Note 1)		I_L = 0 to 8mA	–	0.006	0.010	%/mA

NOTE 1 Line and Load Regulation specifications include the effects of self heating.

NOTE 2 TCV_O is defined as ΔV_{OT} divided by the temperature range, i.e., $TCV_O = \frac{\Delta V_{OT}}{70°C}$

NOTE 3 ΔV_{OT} is defined as the absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range expressed as a percentage of 10V:

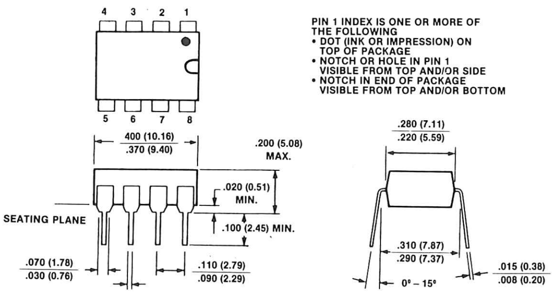
$$\Delta V_{OT} = \frac{V_{MAX}-V_{MIN}}{10V} \times 100$$

Absolute Maximum Ratings

Input Voltage	40V
Power Dissipation	500mW
Derating: To-99, above 80°C ambient Mini Dip, above 30°C ambient	7.1mW/°C 5.6mW/°C
Operating Temperature: 9496 C, D, E, & H	0°C to 70°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

Packaging Information

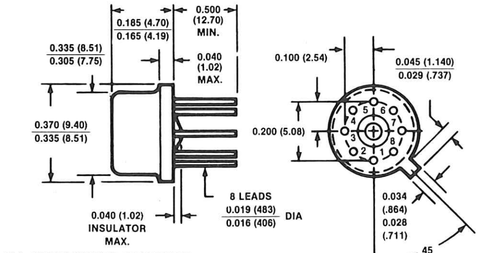
8-PIN PLASTIC MINI-DIP (SUFFIX J)



PIN 1 INDEX IS ONE OR MORE OF THE FOLLOWING
- DOT (INK OR IMPRESSION) ON TOP OF PACKAGE
- NOTCH OR HOLE IN PIN 1 VISIBLE FROM TOP AND/OR SIDE
- NOTCH IN END OF PACKAGE VISIBLE FROM TOP AND/OR BOTTOM

ALL DIMENSIONS IN INCHES.
(ALL DIMENSIONS IN MILLIMETERS)

TO-99 (SUFFIX E)



ALL DIMENSIONS IN INCHES.
(ALL DIMENSIONS IN MILLIMETERS)

BOTTOM VIEW

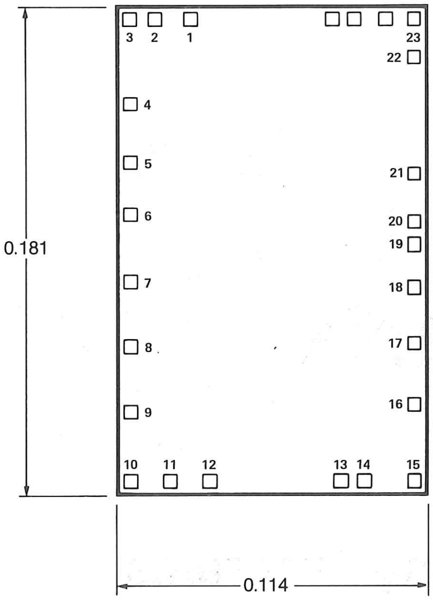
VI
Appendix

- Dice and Bonding Diagrams
- Additional Products by Teledyne Semiconductor
- Glossary of Terms and Abbreviations

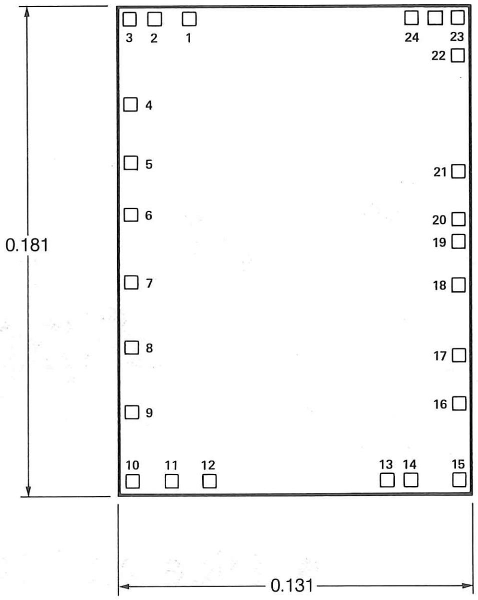
Dice and Bonding Diagrams

These devices are available in dice form. Contact Mt. View for pricing and information. All dimensions in inches.

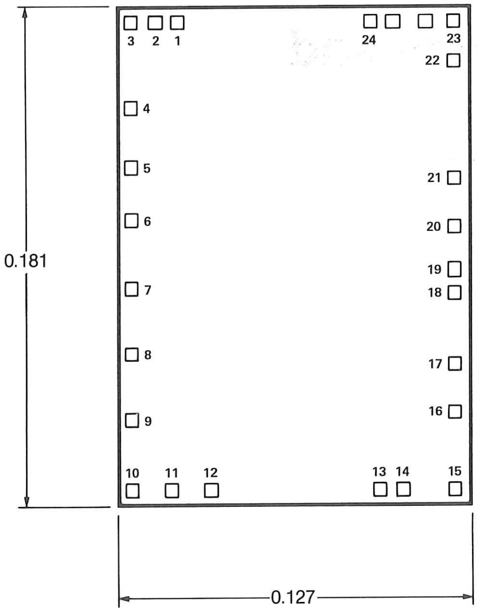
8700, 8701, 8702



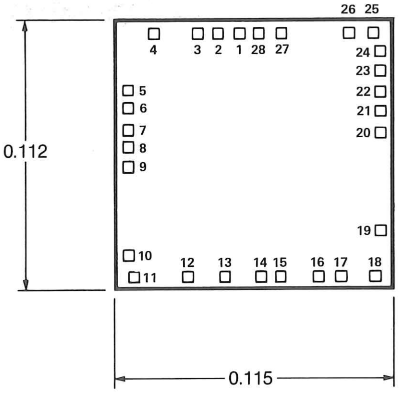
8703, 8704, 8705



8750



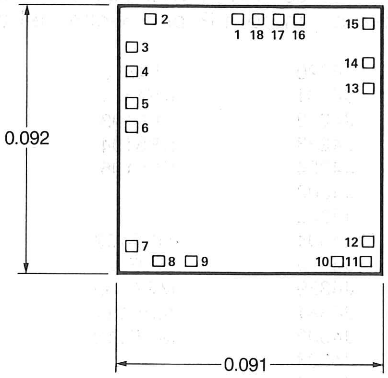
8751



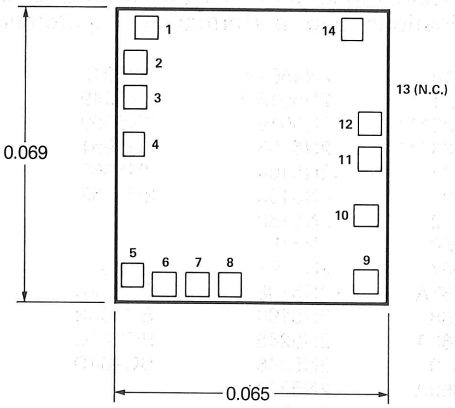
Dice and Bonding Diagrams

These devices are available in dice form. Contact Mt. View for pricing and information. All dimensions in inches.

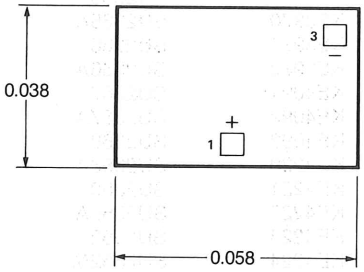
8640, 8641



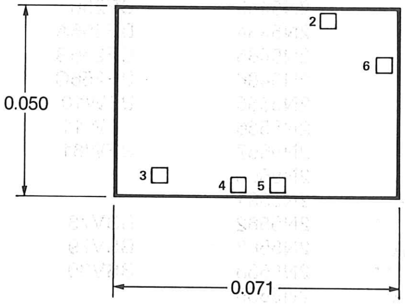
9400



9491



9495, 9496



Additional Products by Teledyne Semiconductor

JFET Products

Teledyne offers junction field effect transistors in both P- and N-channel types, as well as N-channel monolithic duals, to cover a variety of applications and performance requirements.

Amplifiers include RF, HF, VHF, differential and general-purpose types, offering low leakage and low noise figures. Switches are available with low on-resistance, in both P- and N-channel types.

2N3819
2N3821***
2N3822***
2N3823***
2N3824
2N3921
2N3922
2N3966
2N3967
2N3967A
2N3968
2N3968A
2N3969
2N3969A
2N3970
2N3971
2N3972
2N4084
2N4085
2N4091
2N4092
2N4093
2N4220
2N4220A
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2N4221A
2N4222
2N4222A
2N4223
2N4224
2N4302
2N4303
2N4304
2N4338
2N4339
2N4391
2N4392
2N4393
2N4416
2N4416A
2N4856***
2N4856A
2N4857***
2N4857A
2N4858***
2N4858A
2N4859***
2N4859A
2N4860***
2N4860A
2N4861***

2N4861A
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2N5105
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BC264A
BC264B
BC264C
BC264D

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BF245B
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BF247C
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BF256A
BF256B
BF256C
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BFW11
BFW61

BSV78
BSV79
BSV80

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E103
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E111A

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E112A
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E305

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J113
J113A
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J4867RR
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J4868RR
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J4869RR
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J5163

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KE4391
KE4392
KE4393
KE4416
KE4856
KE4857
KE4858
KE4859

KE4860
KE4861
KE5103
KE5104
KE5105

MPF102
MPF108
MPF109
MPF111
MPF112

NF510
NF511

P1086E
P1086RR
P1087E
P1087RR

PAD 20
PAD 50
PAD 100

SU2080
SU2081
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SU2366
SU2366A
SU2367
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SU2656M

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TCR511
TCR512
TCR513

TN5277
TN5278

TP5114
TP5115
TP5116

U200
U201
U202
U231
U232
U233
U234
U235
U308
U309
U310
U1715
U1715A
U1837E
U1837J
U1897E
U1897J
U1898E
U1898J
U1899E
U1899J
U1994E
U1994J
U2047E
U2047J

*** JAN and JANTX Qualified

Additional Products by Teledyne Semiconductor

Digital Products

Digital system designers use Teledyne Semiconductor's Bipolar Interface Logic to improve performance and protection of microprocessor and CMOS circuits, as well as to build complete noise-resistant digital systems. Teledyne's Logic Devices offer guaranteed noise immunity of 3.5V, high output drive (up to 12mA source or 250mA sink) and easy interfacing with other logic types.

Bipolar Interface Logic

Gates

306	Quad 2,2,2,3-Input NOR
307	Quad 2,2,2,3-Input NOR (Open Collector)
321	Quad 2-Input NAND
322	Dual 5-Input NAND
323	Quad 2-Input NAND (Open Collector)
324	Quad 2-Input NAND (Passive Pullup)
325	2,2,3,3-Input NAND
326	2,2,3,3-Input NAND (Passive Pullup)
331	Dual 5-Input Gate Expander
332	Hex Inverter (Open Collector)
333	Hex Inverter (Passive Pullup)
334	Strobed Hex Inverter (Open Collector)
335	Strobed Hex Inverter (Passive Pullup)
341	Dual 2-Input AND-OR-INVERT
344	Dual Expandable AND-NOR

Flip Flops

311	Master/Slave RST
312	Dual J-K Edge Triggered
313	Dual J-K Master/Slave
370	Quad D (Passive Pullup)
375	4-bit Shift Register

Counters

371	Decade (Passive Pullup)
372	Hexadecimal (Passive Pullup)
373	Up/Down Decade
374	Up/Down Hexadecimal

Comparator

343	4-bit Digital Comparator

Decoders/Multiplexers

350	8-bit Multiplexer
351	Dual 4-bit Multiplexer
380	BCD to Decade Decoder/Lamp Driver (Open Collector)
381	BCD to Decade Decoder/Logic Driver (Open Collector)
382	BCD to Decade Decoder/Gas Discharge Driver
383	BCD to Seven Segment Decoder/Driver

One Shots/Timers

342	Dual Monostable Multivibrator
347	Dual Retriggerable Monostable Multivibrator
349	Dual Retriggerable Pulse Stretcher
355	HiNIL Timer

Interface Circuits

361	Dual HiNIL to 5 Volt Interface
362	Dual 5 Volt to HiNIL Interface
363	Quad 5 Volt to HiNIL Interface
367	Quad Schmitt Trigger/Line Receiver
368	Quad Schmitt Trigger/Line Receiver (Open Collector)

Buffer Gates

301	Dual 5-Input Power NAND
302	Quad 2-Input Power NAND (Open Collector)
303	Quad 2-Input Power NAND (Passive Pullup)
304	Triple 4,3,4-Input Power NAND (Passive Pullup)
390	Dual 4-Input AND
391	Dual AND
392	Dual NAND
393	Dual OR
394	Dual NOR
395	Dual 4-Input NAND
396	Dual Line Driver/Receiver

Glossary of Terms and Abbreviations

BCD	Binary Coded Decimal
C_{AZ}	Auto-Zero Storage Capacitance
C_{INT}	Integrator Capacitance
C_L	Load Capacitance
CMR	Common Mode Range
CMRR	Common Mode Rejection Ratio
COMP	Analog Comparator Output
C_{OSC}	Oscillator Capacitance
EOC	End of Conversion Signal
f_{CLK}	Clock Frequency
f_{IN}	Clock Input Frequency
FS	Full Scale
I_{BIAS}	Input Bias Current
I_{DD}	Drain Supply Current
I_{IN}	Input Current
I_{INH}	Logic Input Current, Input Voltage High
I_{INL}	Logic Input Current, Input Voltage Low
I_o	Output Current
I_{OH}	Output Current, Output Voltage High
I_{OL}	Output Current, Output Voltage Low
I_{OS}	Input Offset Current
I_{SC}	Output Short Circuit Current
I_{SS}	Source Supply Current
LSB	Least Significant Bit
MSB	Most Significant Bit
OF	Overflow Logic Output Pulse
OR	Overrange Logic Output Pulse
P_D	Power Dissipation
P–P	Peak to Peak
PSRR	Power Supply Rejection Ratio
$r_{DS(on)}$	ON Resistance of FET Switch
REF_{out}	Reference Output Voltage
R_L	Load Resistance
R_S	Input Source Resistance
S_R	Slew Rate
T_A	Ambient Temperature
TC	Temperature Coefficient
t_r	Response Time
U/D	Up/Down Logic Output
UR	Underrange Logic Output Pulse
V_{AZ}	Auto-Zero Amplifier Output Voltage
V_{DD}	Drain Supply Voltage; Negative for PMOS, Positive for NMOS and CMOS
V_{IN}	Input Voltage
V_{INH}	Logic Input Voltage, High
V_{INL}	Logic Input Voltage, Low
V_O	Output Voltage
V_{OH}	Output Voltage, High
V_{OL}	Output Voltage, Low
V_{OS}	Input Offset Voltage
V_{OUT}	Output Voltage Swing
V_{REF}	Positive Reference Voltage
V_S	Supply Voltage
V_{SS}	Source Supply Voltage; Positive for PMOS, Negative for NMOS and CMOS
Z_{IN}	Input Impedance

DATA CONVERSION ACTION REPLY CARD

TELEDYNE SEMICONDUCTOR

Which Data Conversion Product best suits your need?

A/D

☐ 8-bit ... ☐ with 3-State outputs
☐ 10-bit ... ☐ with 3-State outputs
☐ 12-bit ... ☐ with 3-State outputs
☐ 3½ digit Parallel BCD outputs
☐ 3½ digit Multiplexer BCD outputs
☐ 3½ digit 7 segment LCD output
☐ 3½ digit 7 segment LED output

D/A

☐ 12-bit, ±1%
☐ 12-bit, ±½%

Voltage References

☐ 1.22V
☐ 5.00V
☐ 10.00V

V/F, F/V

☐ V/F converter
☐ F/V converter

Multiplexers

☐ 16 Channel ☐ Dual 8
☐ 7 Channel ☐ Dual 4

In what product will it be used? ____________________
____

Starting when? __________ Usage/Yr? __________
What other data conversion products are you currently using or evaluating? ____________________
____

☐ Please send an evaluation sample.
Part No. ____________________
What features of these products are particularly attractive to you? ____________________
____

Please send a quotation on the following:

Prod. #	Quantity	Deliv. Req.

I would like additional literature on the following Teledyne Semiconductor products:

☐ JFETS — junction field effect transistors
☐ Bipolar Interface Logic (HiNIL)
☐ — Send additional Data Conversion Design Manual
☐ — Add name to mailing list
☐ Other ____________________

Name ____________________
Title ____________________
Company ____________________
Mail Stop ____________________
Address ____________________
City ____________________
State __________ **Zip** __________
Phone (   ) ____________________

DATA CONVERSION ACTION REPLY CARD
TELEDYNE SEMICONDUCTOR

Which Data Conversion Product best suits your need?

A/D

☐ 8-bit ... ☐ with 3-State outputs
☐ 10-bit ... ☐ with 3-State outputs
☐ 12-bit ... ☐ with 3-State outputs
☐ 3½ digit Parallel BCD outputs
☐ 3½ digit Multiplexer BCD outputs
☐ 3½ digit 7 segment LCD output
☐ 3½ digit 7 segment LED output

D/A

☐ 12-bit, ±1%
☐ 12-bit, ±½%

Voltage References

☐ 1.22V
☐ 5.00V
☐ 10.00V

V/F, F/V

☐ V/F converter
☐ F/V converter

Multiplexers

☐ 16 Channel ☐ Dual 8
☐ 7 Channel ☐ Dual 4

In what product will it be used? ____________________
____

Starting when? __________ Usage/Yr? __________
What other data conversion products are you currently using or evaluating? ____________________
____

☐ Please send an evaluation sample.
Part No. ____________________
What features of these products are particularly attractive to you? ____________________
____

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☐ Bipolar Interface Logic (HiNIL)
☐ — Send additional Data Conversion Design Manual
☐ — Add name to mailing list
☐ Other ____________________

Name ____________________
Title ____________________
Company ____________________
Mail Stop ____________________
Address ____________________
City ____________________
State __________ **Zip** __________
Phone (   ) ____________________

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IN THE
UNITED STATES

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1300 Terra Bella Avenue
Mountain View, CA 94043

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Teledyne Semiconductor
1300 Terra Bella Avenue
Mountain View, CA 94043

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Kowloon, Hong Kong, 3-240122

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